# 20-W Stereo Digital Audio Power Amplifier with EQ and DRC

**Check for Samples: TAS5706**

## FEATURES

- **Audio Input/Output**
  - **20-W into an 8-Ω Load From an 18-V Supply**
  - **Two Serial Audio Inputs (Four Audio Channels)**
  - **Supports Multiple Output Configurations:**
    - **2-Ch Bridged Outputs (20 W × 2)**
    - **4-Ch Single-Ended Outputs (10 W × 4)**
    - **2-Ch Single-Ended + 1-Ch Bridged (2.1) (10 W × 2 + 20 W)**
- **Closed Loop Power Stage Architecture**
  - **Improved PSRR Reduces Power Supply Performance Requirements**
  - **Higher Damping Factor Provides for Tighter, More Accurate Sound With Improved Bass Response**
  - **Constant Output Power Over Variation in Supply**
- **Wide PVCC Range From (10 V to 26 V)**
  - **No Separate Supply Required for Gate Drive**
- **Supports 32-kHz–192-kHz Sample Rates (LJ/RJ/I$^2$S)**
- **Headphone PWM Outputs**
- **Subwoofer PWM Outputs**
- **AM Interference Avoidance Support**
- **Audio/PWM Processing**
  - **Independent Channel Volume Controls With 24-dB to –100-dB Range—Soft Mute (50% Duty Cycle)**
  - **Programmable Dynamic Range Control**
  - **16 Programmable Biquads for Speaker Equalization**
  - **Adaptive Biquad Coefficients for EQ and DRC Filters**
  - **Programmable Input and Output Mixers**
  - **Loudness Compensation for Subwoofer**
  - **Automatic Sample-Rate Detection and Coefficient Banking**
- **General Features**
  - **Serial Control Interface Operational Without MCLK**
  - **Factory-Trimmed Internal Oscillator Avoids the Need for External Crystal**
  - **Surface Mount, 64-Terminal, 10-mm × 10-mm HTQFP Package**
  - **Thermal and Short-Circuit Protection**

## DESCRIPTION

The TAS5706 is a 20-W, efficient, digital audio power amplifier for driving stereo bridged-tied speakers. Two serial data inputs allow processing of up to four discrete audio channels and seamless integration to most digital audio processors and MPEG decoders, accepting a wide range of input data and clock rates. A fully programmable data path allows these channels to be routed to the internal speaker drivers or output via the subwoofer or headphone PWM outputs.

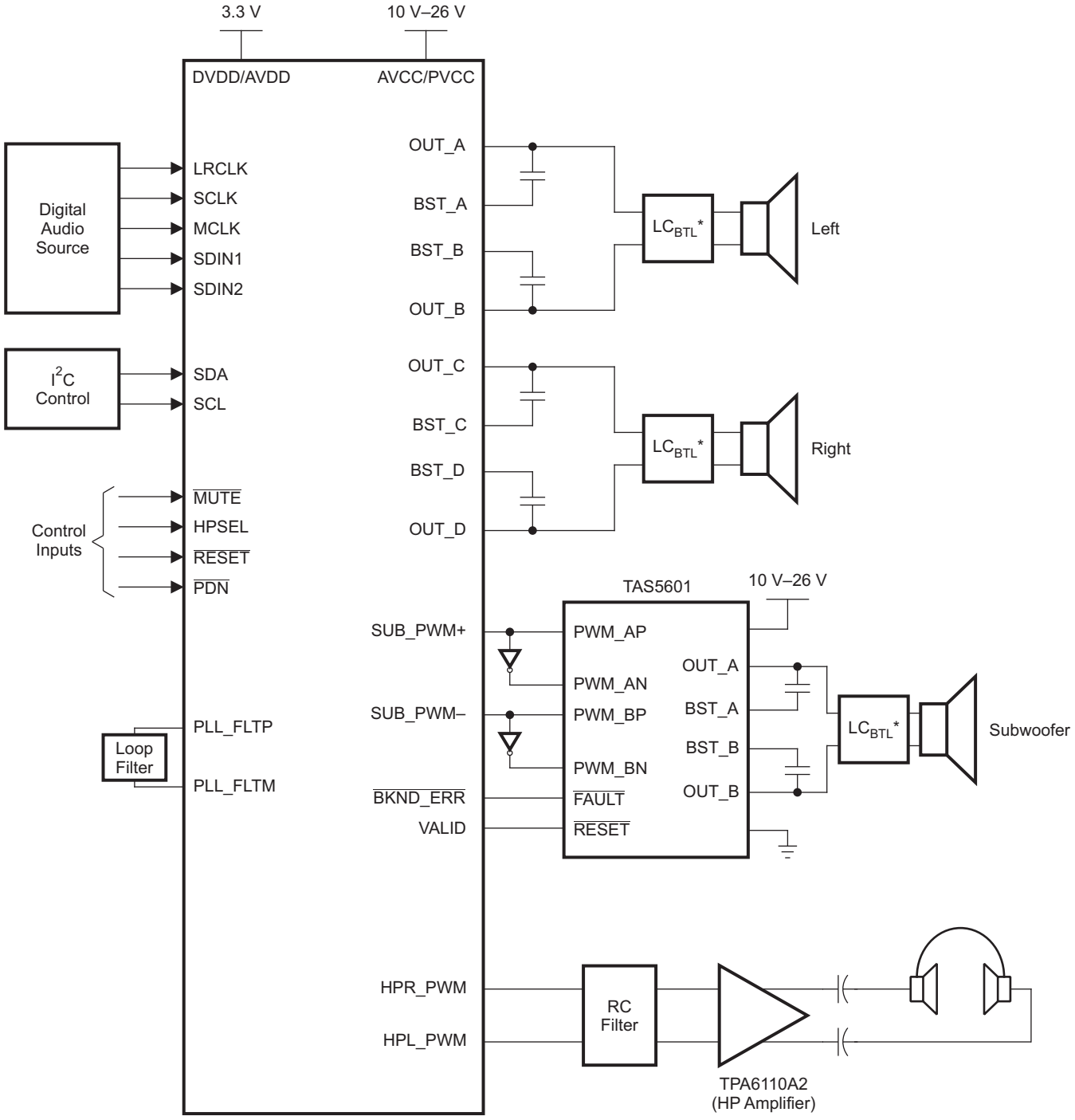
The TAS5706 is a slave-only device receiving all clocks from external sources. The TAS5706 operates at a 384-kHz switching rate for 32-, 48-, 96-, and 192-kHz data, and at a 352.8 kHz switching rate for 44.1-, 88.2-, and 176.4-kHz data. The 8× oversampling combined with the fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## SIMPLIFIED APPLICATION DIAGRAMS

### Bridge-Tied Load (BTL) Mode




* Refer to TI Application Note (SLOA119) on LC filter design for BTL (AD/BD mode) configuration.

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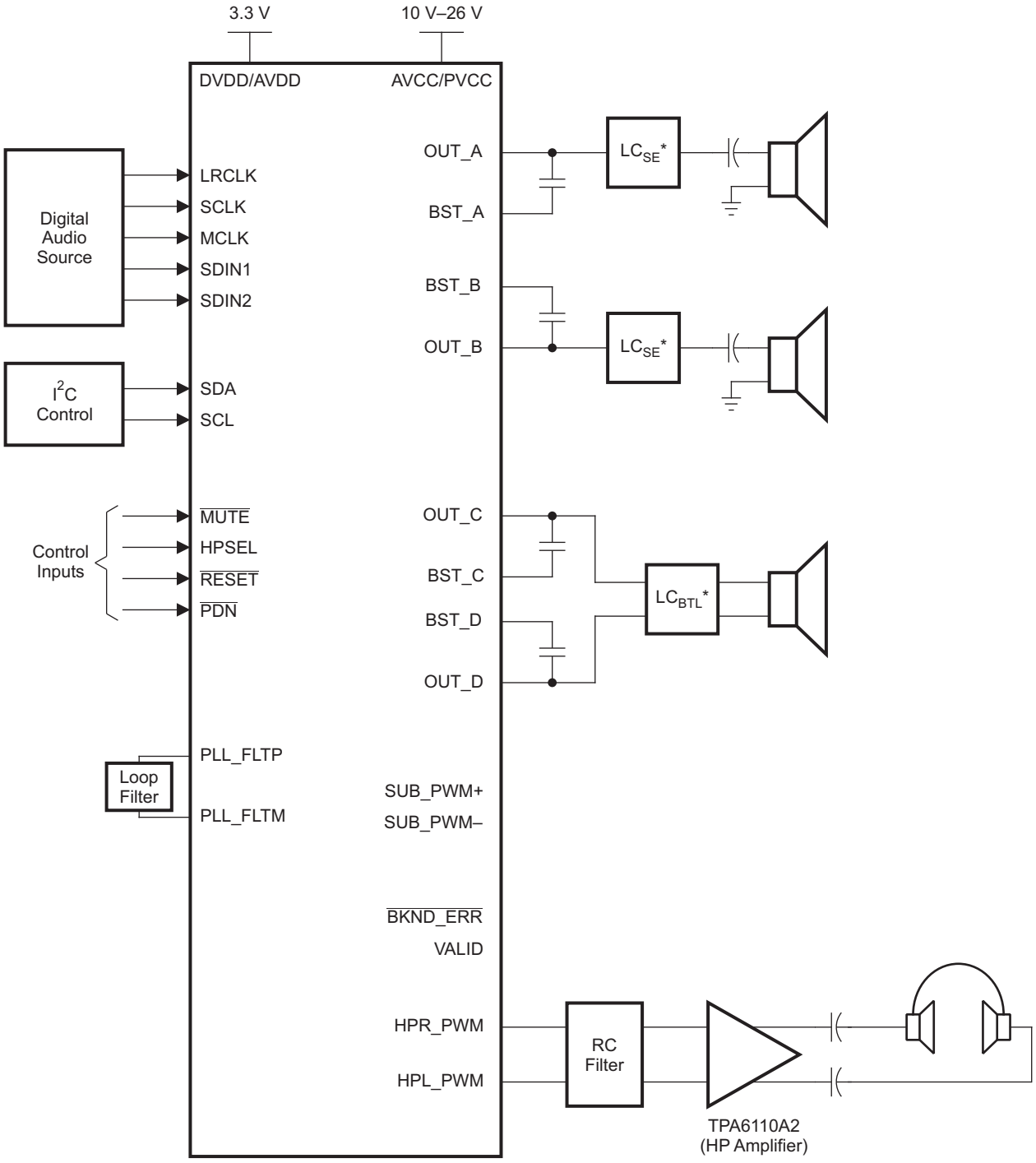
### Single-Ended (SE) 2.1 Mode




* Refer to TI Application Note (SLOA119) on LC filter design for SE or BTL configuration.

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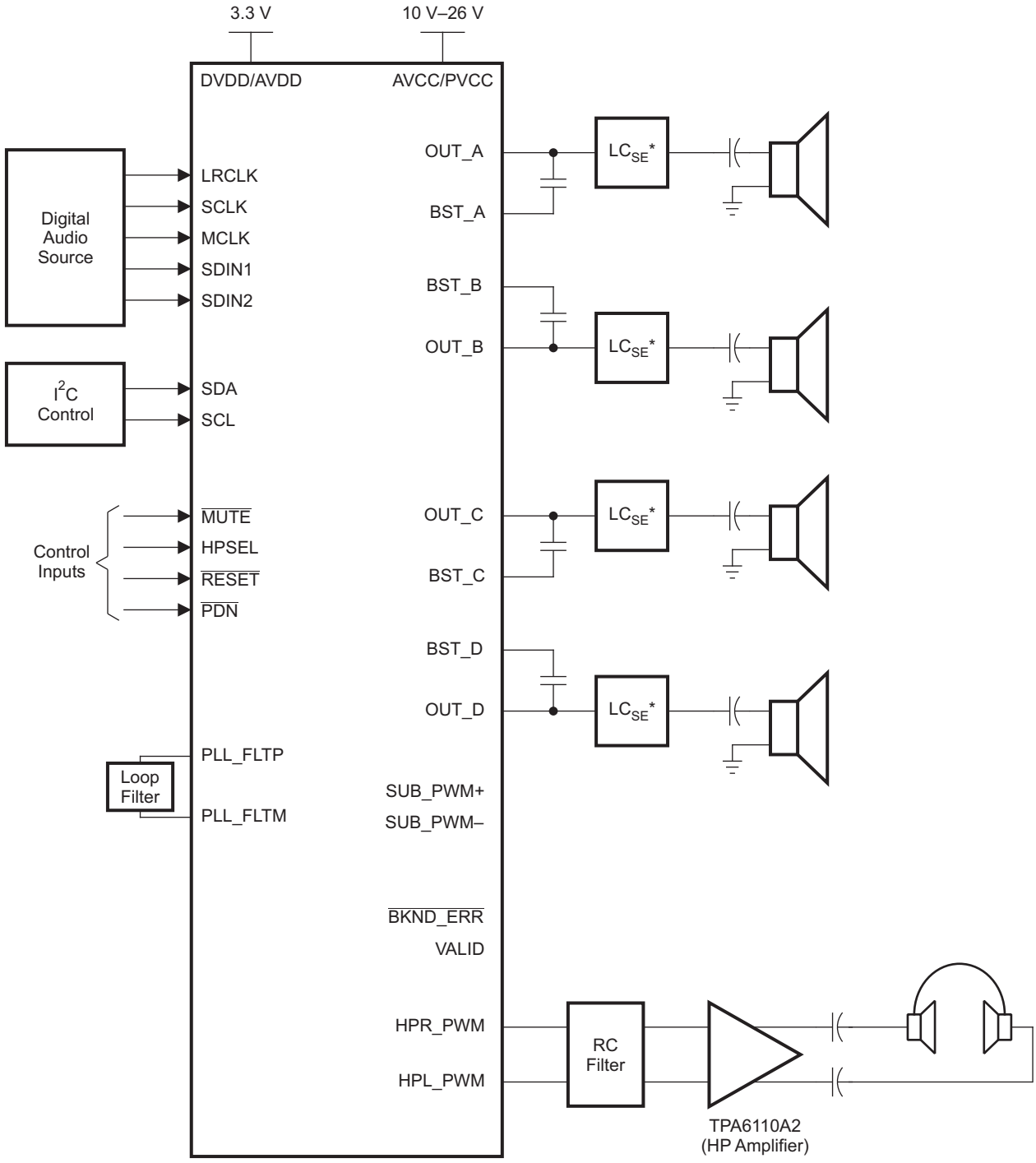
### Single-Ended (SE) 4.0 Mode




* Refer to TI Application Note (SLOA119) on LC filter design for SE configuration.

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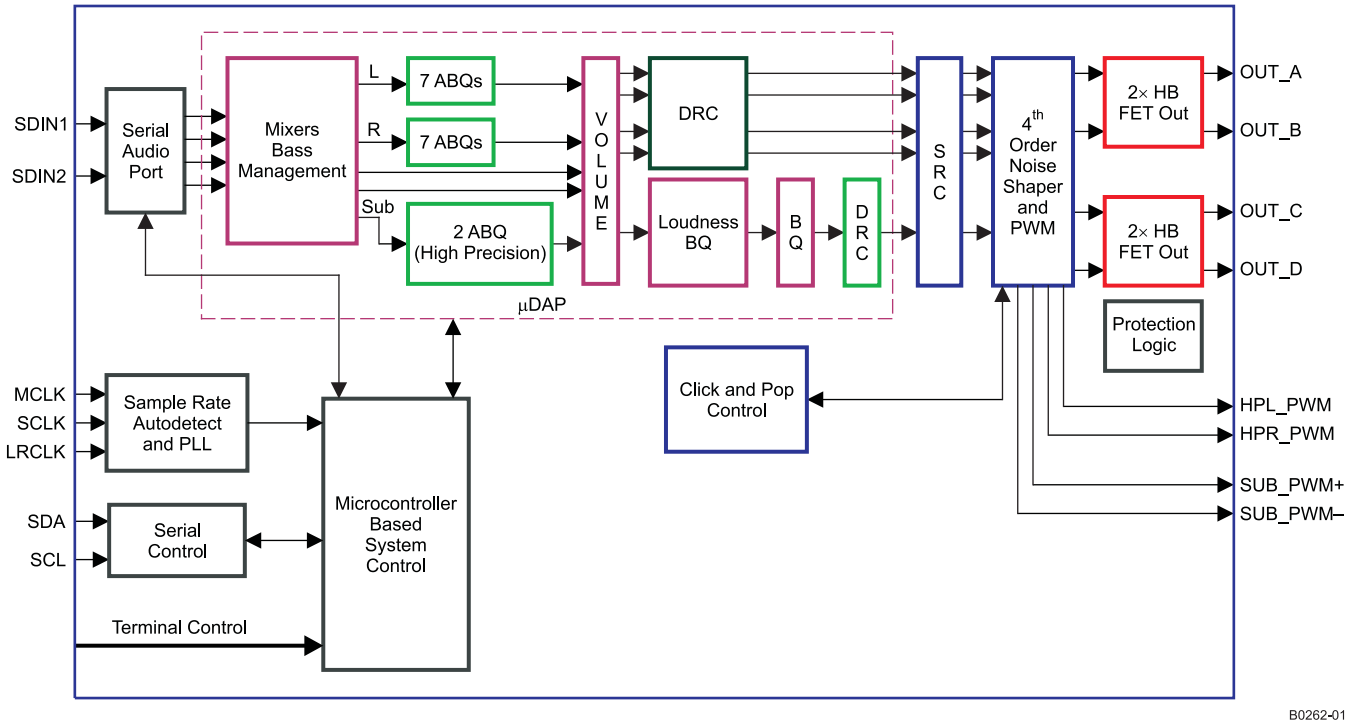
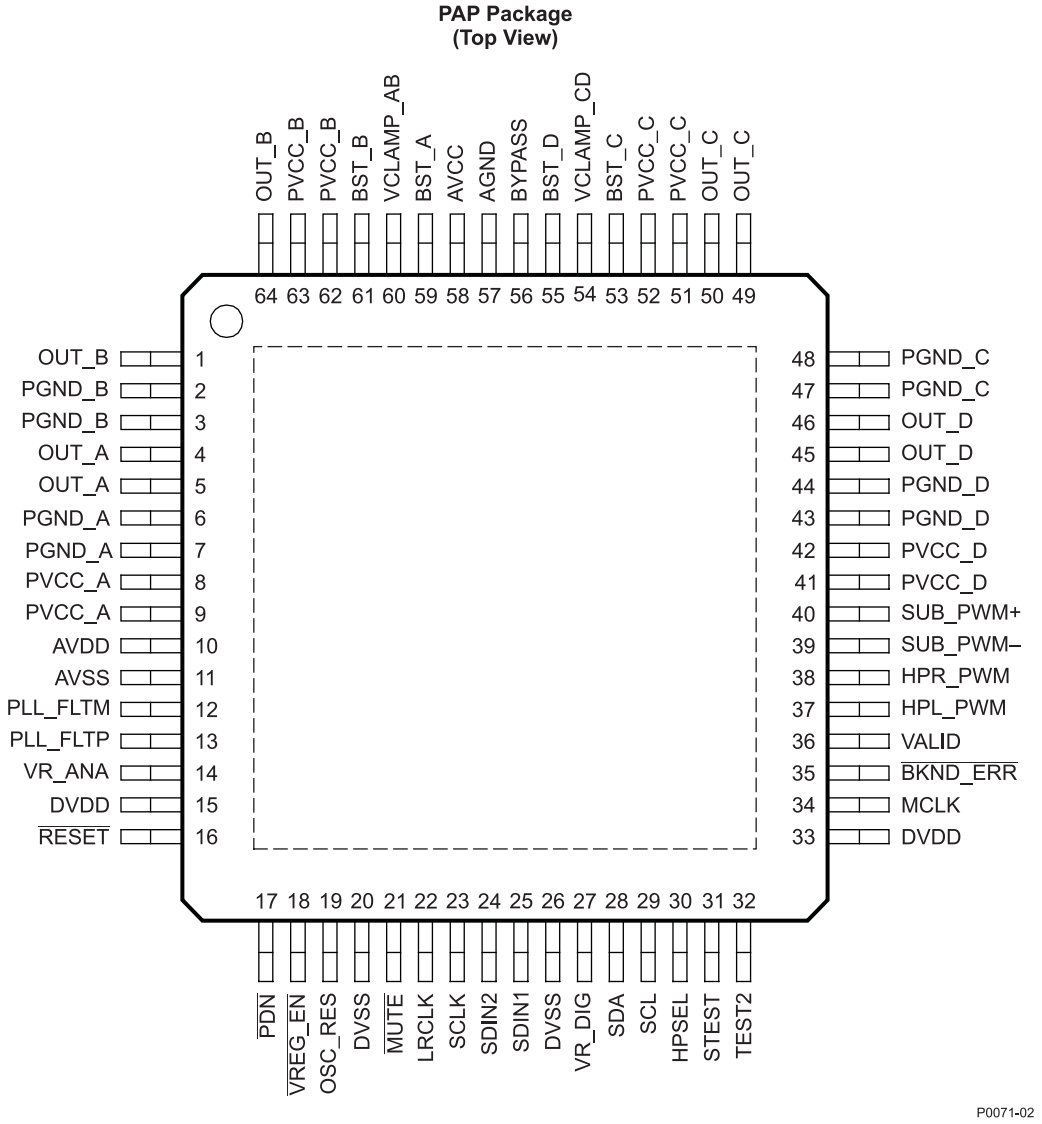
## FUNCTIONAL VIEW



## 64-TERMINAL, HTQFP PACKAGE (TOP VIEW)




### TERMINAL FUNCTIONS

| TERMINAL | | TYPE (1) | 5-V TOLERANT | TERMINATION (2) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| AGND | 57 | P | | | Analog ground for power stage |
| AVCC | 58 | P | | | Analog power supply for power stage. Connect externally to same potential as PVCC. |
| AVDD | 10 | P | | | 3.3-V analog power supply. DVDD and AVDD must ramp up together with voltage difference restricted to no more than 0.4 V. |
| AVSS | 11 | P | | | Analog 3.3-V supply ground |
| BKND_ERR | 35 | DI | | Pullup | Active-low. A back-end error sequence is generated by applying logic LOW to this terminal. This terminal is connected to an external power stage. If no external power stage is used, connect this terminal directly to DVDD. |

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2) All pullups are 20-μA weak pullups and all pulldowns are 20-μA weak pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input). Devices that drive inputs with pullups must be able to sink 20 μA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 20 μA while maintaining a logic-1 drive level.

## TERMINAL FUNCTIONS (continued)

| TERMINAL | | TYPE (1) | 5-V TOLERANT | TERMINATION (2) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| BST_A | 59 | P | | | High-side bootstrap supply for half-bridge A |
| BST_B | 61 | P | | | High-side bootstrap supply for half-bridge B |
| BST_C | 53 | P | | | High-side bootstrap supply for half-bridge C |
| BST_D | 55 | P | | | High-side bootstrap supply for half-bridge D |
| BYPASS | 56 | O | | | Nominally equal to $V_{CC}/8$. Internal reference voltage for analog cells |
| DVDD | 15, 33 | P | | | 3.3-V digital power supply. DVDD and AVDD must ramp up together with voltage difference restricted to no more than 0.4 V. |
| DVSS | 20, 26 | P | | | Digital ground |
| HPL_PWM | 37 | DO | | | Headphone left-channel PWM output. |
| HPR_PWM | 38 | DO | | | Headphone right-channel PWM output. |
| HPSEL | 30 | DI | 5-V | | Headphone select, active high. When a logic HIGH is applied, device enters headphone mode and speakers are HARD MUTED. When a logic LOW is applied, device is in speaker mode and headphone outputs become line outputs or are disabled. |
| LRCLK | 22 | DI | 5-V | | Input serial audio data left/right clock (sampling rate clock) |
| MCLK | 34 | DI | 5-V | | MCLK is the clock master input. The input frequency of this clock can range from 4.9 MHz to 49 MHz. |
| $\overline{\text{MUTE}}$ | 21 | DI | 5-V | Pullup | Performs a soft mute of outputs, active-low. A logic low on this terminal sets the outputs equal to 50% duty cycle. A logic high on this terminal allows normal operation. The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume. |
| OSC_RES | 19 | AO | | | Oscillator trim resistor. Connect an 18.2-kΩ resistor to GND. |
| OUT_A | 4, 5 | O | | | Output, half-bridge A |
| OUT_B | 1, 64 | O | | | Output, half-bridge B |
| OUT_C | 49, 50 | O | | | Output, half-bridge C |
| OUT_D | 45, 46 | O | | | Output, half-bridge D |
| $\overline{\text{PDN}}$ | 17 | DI | 5-V | Pullup | Power down, active-low. $\overline{\text{PDN}}$ powers down all logic, stops all clocks, and outputs stops switching. When $\overline{\text{PDN}}$ is released, the device powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration determined by register settings. |
| PGND_A | 6, 7 | P | | | Power ground for half-bridge A |
| PGND_B | 2, 3 | P | | | Power ground for half-bridge B |
| PGND_C | 47, 48 | P | | | Power ground for half-bridge C |
| PGND_D | 43, 44 | P | | | Power ground for half-bridge D |
| PLL_FLTM | 12 | AO | | | PLL negative input |
| PLL_FLTP | 13 | AI | | | PLL positive input |
| PVCC_A | 8, 9 | P | | | Power supply input for half-bridge output A |
| PVCC_B | 62, 63 | P | | | Power supply input for half-bridge output B |
| PVCC_C | 51, 52 | P | | | Power supply input for half-bridge output C |
| PVCC_D | 41, 42 | P | | | Power supply input for half-bridge output D |

## TERMINAL FUNCTIONS (continued)

| TERMINAL | | TYPE (1) | 5-V TOLERANT | TERMINATION (2) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| $\overline{\text{RESET}}$ | 16 | DI | 5-V | Pullup | Reset, active-low. A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the DAP to its default conditions, sets the VALID outputs low, and places the PWM in the hard-mute state (stops switching). Master volume is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4- to 5-ms device initialization and sets the volume at mute. |
| SCL | 29 | DI | 5-V | | $I^2C$ serial control clock input |
| SCLK | 23 | DI | 5-V | | Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock. |
| SDA | 28 | DIO | 5-V | | $I^2C$ serial control data interface input/output |
| SDIN1 | 25 | DI | 5-V | | Serial audio data-1 input is one of the serial data input ports. SDIN1 supports three discrete (stereo) data formats. |
| SDIN2 | 24 | DI | 5-V | | Serial audio data-2 input is one of the serial data input ports. SDIN2 supports three discrete (stereo) data formats. |
| STEST | 31 | DI | | | Test terminal. Connect directly to GND. |
| SUB_PWM– | 39 | DO | | | Subwoofer negative PWM output |
| SUB_PWM+ | 40 | DO | | | Subwoofer positive PWM output |
| TEST2 | 32 | DI | | | Test terminal. Connect directly to DVDD. |
| VALID | 36 | DO | | | Output indicating validity of ALL PWM channels, active-high. This terminal is connected to an external power stage. If no external power stage is used, leave this terminal floating. |
| VCLAMP_AB | 60 | P | | | Internally generated voltage supply for channels A and B gate drive. Not to be used as a supply or connected to any component other than the decoupling capacitor |
| VCLAMP_CD | 54 | P | | | Internally generated voltage supply for channels C and D gate drive. Not to be used as a supply or connected to any component other than the decoupling capacitor |
| VR_ANA | 14 | P | | | Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices. |
| VR_DIG | 27 | P | | | Internally regulated 1.8-V digital supply voltage. This terminal must not be used to power external devices. |
| $\overline{\text{VREG\_EN}}$ | 18 | DI | | Pulldown | Voltage regulator enable. Connect directly to GND. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage | DVDD, AVDD | –0.3 to 3.6 | V |
| | PVCC | -0.3 to 30 | V |
| Input voltage | 3.3-V digital input | –0.5 to DVDD + 0.5 | V |
| | 5-V tolerant(2) digital input | –0.5 to DVDD + 2.5 | V |
| Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > 1.8 V | | ±20 | mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > 1.8 V | | ±20 | mA |
| Operating free-air temperature | | 0 to 85 | °C |
| Operating junction temperature range | | 0 to 150 | °C |
| Storage temperature range, $T_{stg}$ | | –40 to 125 | °C |

(1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDA, SCL, and HPSEL.

## DISSIPATION RATINGS

| PACKAGE(1) | DERATING FACTOR | $T_A$ = 25°C POWER RATING | $T_A$ = 45°C POWER RATING | $T_A$ = 70°C POWER RATING |
|---|---|---|---|---|
| 10-mm × 10-mm QFP | 29 mW/°C | 2.89 W | 2.31 W | 1.59 W |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Digital/analog supply voltage | DVDD | 3 | 3.3 | 3.6 | V |
| | Half-bridge supply voltage | PVCC_xx | 10 | | 26 | V |
| $V_{IH}$ | High-level input voltage | 3.3-V TTL, 5-V tolerant | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 3.3-V TTL, 5-V tolerant | | | 0.8 | V |
| $T_A$ | Operating ambient temperature range | | 0 | | 85 | °C |
| $T_J$ | Operating junction temperature range | | 0 | | 150 | °C |
| $R_L$ (BTL) | Load impedance | Output filter: L = 22 μH, C = 680 nF. | 6.0 | 8 | | Ω |
| $R_L$ (SE) | | | 3.2 | 4 | | |
| $R_L$ (PBTL) | | | 3.2 | 4 | | |
| $L_O$ (BTL) | Output-filter inductance | Minimum output inductance under short-circuit condition | | 10 | | μH |
| $L_O$ (SE) | | | | 10 | | |
| $L_O$ (PBTL) | | | | 10 | | |

## PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

| PARAMETER | TEST CONDITIONS | MODE | VALUE | UNITS |
|---|---|---|---|---|
| Output sample rate 2×–1× oversampled | 32–kHz data rate ±2% | 12× sample rate | 384 | kHz |
| | 44.1-, 88.2-, 176.4-kHz data rate ±2% | 8×, 4×, and 2× sample rates | 352.8 | kHz |
| | 48-, 96-, 192-kHz data rate ±2% | 8×, 4×, and 2× sample rates | 384 | kHz |

## PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{MCLKI}$ | Frequency, MCLK (1 / $t_{cyc2}$) | | 4.9 | | 49 | MHz |
| | MCLK duty cycle | | 40% | 50% | 60% | |
| | MCLK minimum high time | ≥2-V MCLK = 49.152 MHz, within the min and max duty cycle constraints | 8 | | | ns |
| | MCLK minimum low time | ≤0.8-V MCLK = 49.152 MHz, within the min and max duty cycle constraints | 8 | | | ns |
| | LRCLK allowable drift before LRCLK reset | | | | 10 | MCLKs |
| | External PLL filter capacitor C1 | SMD 0603 Y5V | | 47 | | nF |
| | External PLL filter capacitor C2 | SMD 0603 Y5V | | 4.7 | | nF |
| | External PLL filter resistor R | SMD 0603, metal film | | 470 | | Ω |

## ELECTRICAL CHARACTERISTICS

DC Characteristics, $T_A$ = 25°C, PVCC_X, AVCC = 18 V, $R_L$ = 8 Ω (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | 3.3-V TTL and 5-V tolerant (1) | $I_{OH}$ = –4 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | 3.3-V TTL and 5-V tolerant (1) | $I_{OL}$ = 4 mA | | | 0.5 | V |
| \| VOS \| | Class-D output offset voltage | | | | ±26 | | mV |
| $V_{BYPASS}$ | PVCC/8 reference for analog section | | No load | 2.2 | 2.26 | 2.3 | V |
| $I_{IL}$ | Low-level input current | 3.3-V TTL | $V_I = V_{IL}$ | | | ±2 | μA |
| | | 5-V tolerant(1) | $V_I$ = 0 V, DVDD = 3 V | | | ±2 | |
| $I_{IH}$ | High-level input current | 3.3-V TTL | $V_I = V_{IH}$ | | | ±2 | μA |
| | | 5-V tolerant | $V_I$ = 5.5 V, DVDD = 3 V | | | ±20 | |
| $I_{DD}$ | Input supply current | Supply voltage (DVDD, AVDD) | Normal mode | 43 | 65 | 80 | mA |
| | | | Power down ($\overline{PDNZ}$ = LOW) | 2 | 8 | 16 | |
| | | | Reset ($\overline{RESET}$ = LOW) | 11 | 23 | 33 | |
| $I_{CC}$ | Quiescent supply current | | No load | 14 | 33 | 57 | mA |
| $I_{CC(\overline{RESET})}$ | Quiescent supply current in reset mode | | No load | | 58 | 176 | μA |
| $I_{CC(\overline{PDNZ})}$ | Quiescent supply current in power down mode | | No load | | 58 | 176 | μA |
| PSRR | DC power-supply rejection ratio | | PVCC = 17.5 V to 18.5 V | | 60 | | dB |
| $R_{DS(on)}$ | Drain-source on-state resistance, high-side | | $V_{CC}$ = 18 V , $I_O$ = 500 mA, $T_J$ = 25°C | | 240 | | mΩ |
| | Low-side | | | | 240 | | |
| | Total | | | | 480 | 850 | |
| $t_{ON}$ | Turnon time (SE mode) (Set Reg 0x1A bit 7 to 1) | | $C_{(BYPASS)}$ = 1 μF, Time required for the $C_{(BYPASS)}$ to reach its final value | | 500 | | ms |
| | Turnon time (BTL mode) (Set Reg 0x1A bit 7 to 0) | | | | 30 | | |
| $t_{OFF}$ | Turnoff time (SE mode) (Set Reg 0X1A bit 7 to 1) | | | | 500 | | ms |
| | Turnoff time (BTL mode) (Set Reg 0X1A bit 7 to 0) | | | | 30 | | |

(1) 5-V tolerant pins are $\overline{PDN}$, $\overline{RESET}$, $\overline{MUTE}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDA, SCL, and HPSEL.

## AC Characteristics, $T_A$ = 25°C, PVCC_X, AVCC = 18 V, AVDD, DVDD = 3.3 V, $R_L$ = 8 Ω (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| KSVR | Supply ripple rejection | 100-$mV_{PP}$ ripple at 20 Hz–20 kHz, BTL, 50% duty cycle PWM | | –60 | | dB |
| $P_O$ | Continuous output power | BTL ($R_L$ = 8 Ω, THD+N = 10%, f = 1 kHz, PVCC = 18 V) | | 20.6 | | W |
| | | BTL ($R_L$ = 8 Ω, THD+N = 7%, f = 1 kHz, PVCC = 18 V) | | 19.3 | | W |
| | | SE ($R_L$ = 4 Ω, THD+N = 10%, f = 1 kHz, PVCC = 24 V) | | 18.1 | | W |
| | | SE ($R_L$ = 4 Ω, THD+N = 7%, f = 1 kHz, PVCC = 24 V) | | 17.3 | | W |
| THD+N | Total harmonic distortion + noise (SE) | $V_{CC}$ = 24 V, $R_L$ = 4 Ω, f = 1 kHz, $P_O$ = 10 W (half-power) | | 0.08% | | |
| | Total harmonic distortion + noise (BTL) | $V_{CC}$ = 18 V, $R_L$ = 8 Ω, f = 1 kHz, $P_O$ = 10 W (half-power) | | 0.05% | | |
| $V_n$ | Output integrated noise | 20 Hz to 22 kHz (BD mode) | | 115 | | μV |
| | | A-weighted filter; $\overline{MUTE}$ = LOW | | –82 | | dBV |
| Crosstalk | | $P_O$ = 1 W, f = 1 kHz | | –69 | | dB |
| SNR | Signal-to-noise ratio | Maximum output at THD+N < 1%, f = 1 kHz, A-weighted | | 99 | | dB |
| | Thermal trip point (output shutdown, unlatched fault) | | | 150 | | °C |
| | Thermal hysteresis | | | 15 | | °C |

(1) All measurement in AD mode.

## AC Characteristics, $T_A$ = 25°C, PVCC_X, AVCC = 12 V, AVDD, DVDD = 3.3 V, $R_L$ = 8 Ω (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| KSVR | Supply ripple rejection | 100-mVpp ripple at 20 Hz–20 kHz, BTL, 50% duty cycle PWM | | –60 | | dB |
| $P_O$ | Continuous output power | BTL ($R_L$ = 8 Ω, THD+N = 10%, f = 1 kHz) | | 9.2 | | W |
| | | BTL ($R_L$ = 8 Ω, THD+N = 7%, f = 1 kHz) | | 8.7 | | W |
| | | SE ($R_L$ = 4 Ω, THD+N = 10%, f = 1 kHz) | | 4.5 | | W |
| | | SE ($R_L$ = 4 Ω, THD+N = 7%, f = 1 kHz) | | 4.2 | | W |
| THD+N | Total harmonic distortion + noise (BTL) | $V_{CC}$ = 12 V, $R_L$ = 8 Ω, f = 1 kHz, $P_O$ = 5 W (half-power) | | 0.07% | | |
| $V_n$ | Output integrated noise | 20 Hz to 22 kHz (BD mode) | | 115 | | μV |
| | | A-weighted filter | | –82 | | dBV |
| Crosstalk | | $P_O$ = 1 W, f = 1 kHz | | –75 | | dB |
| SNR | Signal-to-noise ratio | Maximum output at THD+N < 1%, f = 1 kHz, A-weighted | | 96 | | dB |
| | Thermal trip point (output shutdown, unlatched fault) | | | 150 | | °C |
| | Thermal hysteresis | | | 15 | | °C |

(1) All measurement in AD mode.

## SERIAL AUDIO PORTS SLAVE MODE

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCLKIN}$ | Frequency, SCLK 32 × $f_S$, 48 × $f_S$, 64 × $f_S$ | $C_L$ = 30 pF | 1.024 | | 12.288 | MHz |
| $t_{su1}$ | Setup time, LRCLK to SCLK rising edge | | 10 | | | ns |
| $t_{h1}$ | Hold time, LRCLK from SCLK rising edge | | 10 | | | ns |
| $t_{su2}$ | Setup time, SDIN to SCLK rising edge | | 10 | | | ns |
| $t_{h2}$ | Hold time, SDIN from SCLK rising edge | | 10 | | | ns |
| | LRCLK frequency | | 32 | 48 | 192 | kHz |
| | SCLK duty cycle | | 40% | 50% | 60% | |
| | LRCLK duty cycle | | 40% | 50% | 60% | |
| | SCLK rising edges between LRCLK rising edges | | 32 | | 64 | SCLK edges |
| $t_{(edge)}$ | LRCLK clock edge with respect to the falling edge of SCLK | | –1/4 | | 1/4 | SCLK period |

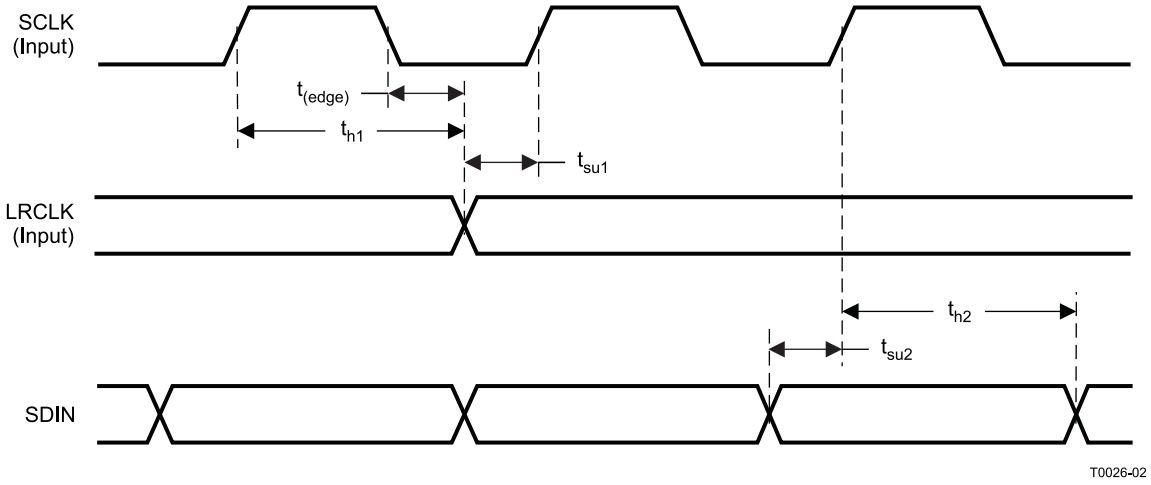



**Figure 1. Slave Mode Serial Data Interface Timing**

## I²C SERIAL CONTROL PORT OPERATION

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | Frequency, SCL | No wait states | | 400 | kHz |
| $t_{w(H)}$ | Pulse duration, SCL high | | 0.6 | | μs |
| $t_{w(L)}$ | Pulse duration, SCL low | | 1.3 | | μs |
| $t_r$ | Rise time, SCL and SDA | | | 300 | ns |
| $t_f$ | Fall time, SCL and SDA | | | 300 | ns |
| $t_{su1}$ | Setup time, SDA to SCL | | 100 | | ns |
| $t_{h1}$ | Hold time, SCL to SDA | | 0 | | ns |
| $t_{(buf)}$ | Bus free time between stop and start condition | | 1.3 | | μs |
| $t_{su2}$ | Setup time, SCL to start condition | | 0.6 | | μs |
| $t_{h2}$ | Hold time, start condition to SCL | | 0.6 | | μs |
| $t_{su3}$ | Setup time, SCL to stop condition | | 0.6 | | μs |
| $C_L$ | Load capacitance for each bus line | | | 400 | pF |

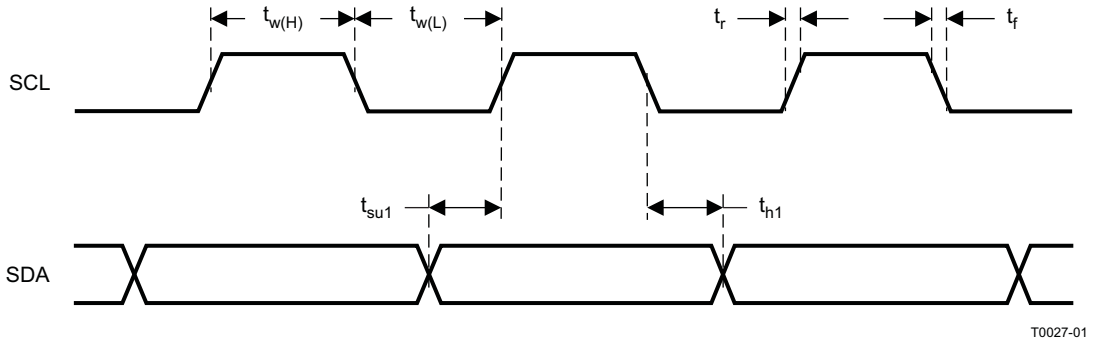



**Figure 2. SCL and SDA Timing**

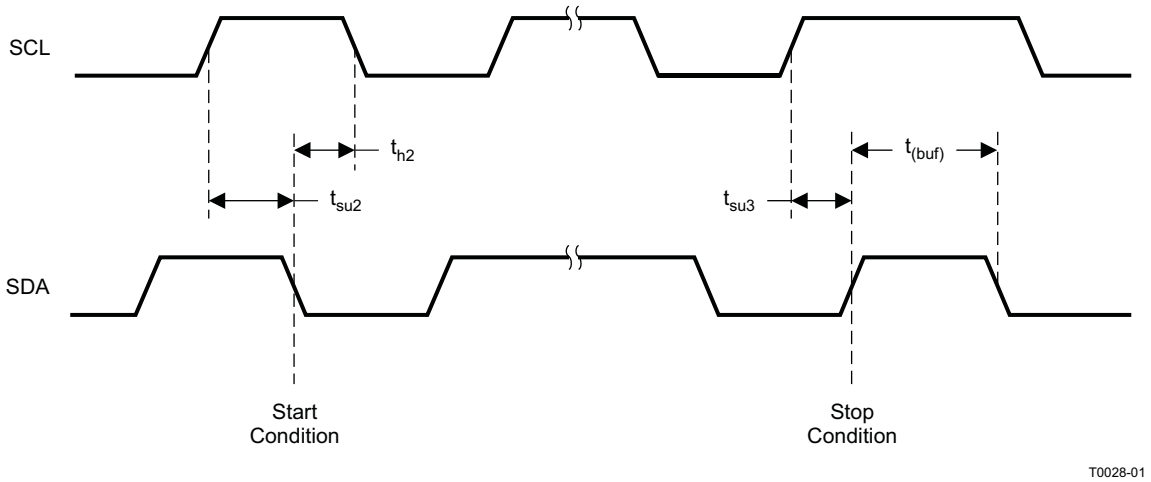
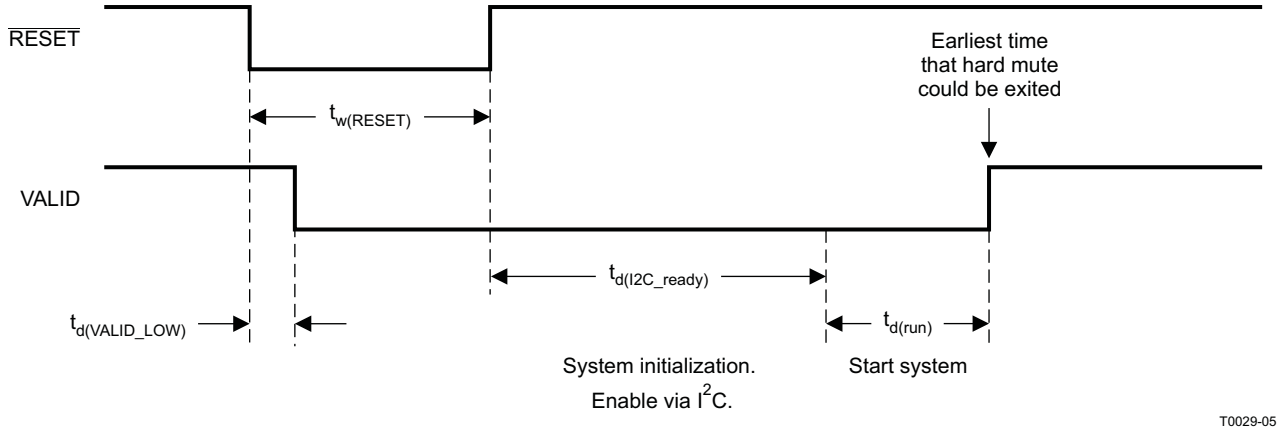



**Figure 3. Start and Stop Conditions Timing**

## RESET TIMING ($\overline{\text{RESET}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(VALID\_LOW)}$ | Time to assert VALID (reset to power stage) low | | 300 | | ns |
| $t_{w(RESET)}$ | Pulse duration, $\overline{\text{RESET}}$ active | | 1 | | ms |
| $t_{d(I2C\_ready)}$ | Time to enable $I^2C$ | | 3.5 | | ms |
| $t_{d(run)}$ | Device start-up time (after start-up command via $I^2C$) | 10 | | | ms |



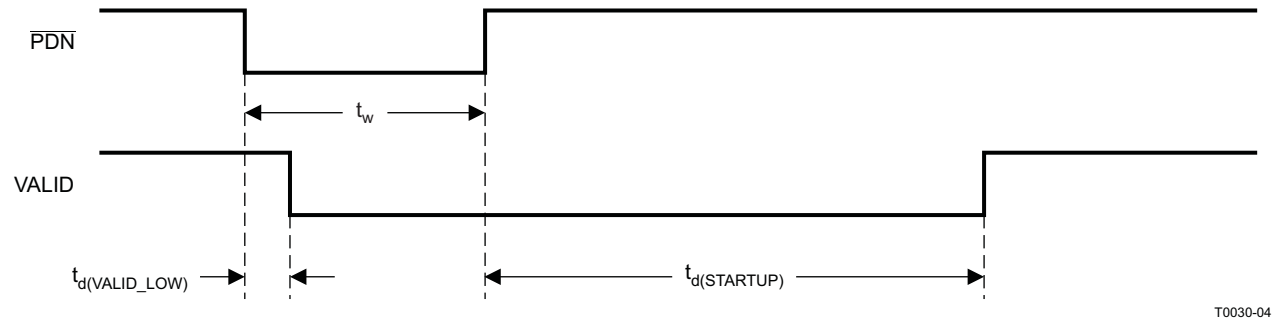

NOTE: On power up, it is recommended that the TAS5706 $\overline{\text{RESET}}$ be held LOW for at least 100 μs after DVDD has reached 3.0 V. RESET assertion is ignored if applied while part is powered down

**Figure 4. Reset Timing**

## POWER-DOWN ($\overline{\text{PDN}}$) TIMING

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(VALID\_LOW)}$ | Time to assert VALID (reset to power stage) low | | 725 | | μs |
| $t_{d(STARTUP)}$ | Device startup time | | 120 | | ms |
| $t_w$ | Minimum pulse duration required | | 800 | | ns |




NOTE: PDNZ assertion is ignored if applied when part is in RESET

**Figure 5. Power-Down Timing**

## BACK-END ERROR ($\overline{\text{BKND\_ERR}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(ER)}$ | Pulse duration, $\overline{\text{BKND\_ERR}}$ active (active-low) | | 350 | None | ns |

## BACK-END ERROR ($\overline{\text{BKND\_ERR}}$) (continued)

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{p(valid\_high)}$ | Programmable. Time to stay in the OUT_x low state. After $t_{p(valid\_high)}$, the TAS5706 attempts to bring the system out of the OUT_x low state if $\overline{\text{BKND\_ERR}}$ is high. Refer Reg 0x1C | | | | ms |
| $t_{p(valid\_low)}$ | Time TAS5706 takes to bring OUT_x low after $\overline{\text{BKND\_ERR}}$ assertion. | | 350 | | ns |

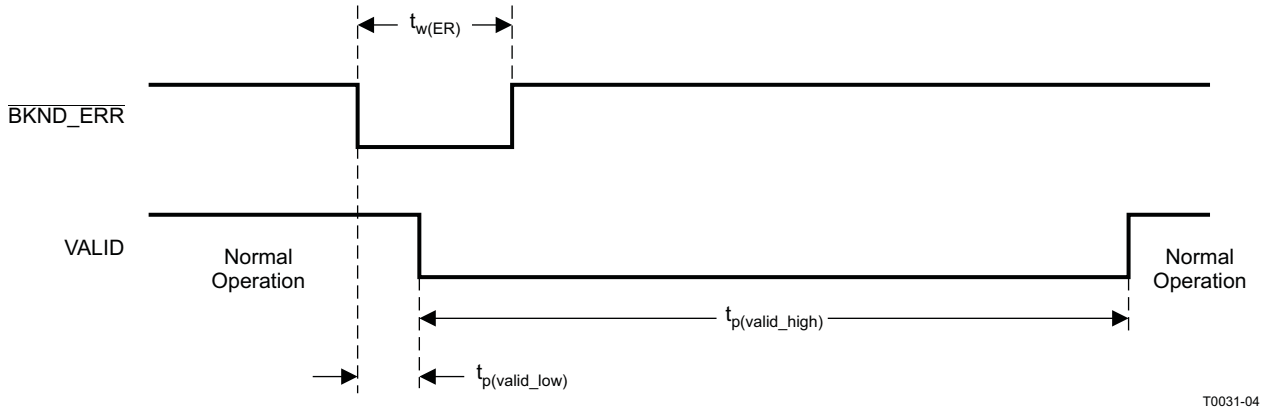



**Figure 6. Error Recovery Timing**

## MUTE TIMING ($\overline{\text{MUTE}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{d(VOL)}$ | Volume ramp time. Ramp Time = Number of Steps (programmable number of steps, refer register 0x0E) × Stepsize (1) | | 1024 | | steps |

(1) Stepsize = 4 LRCLKs (for 32–48 kHz sample rate); 8 LRCLKs (for 88.2–96 kHz sample rate); 16 LRCLKs (for 176.4–192 kHz sample rate)

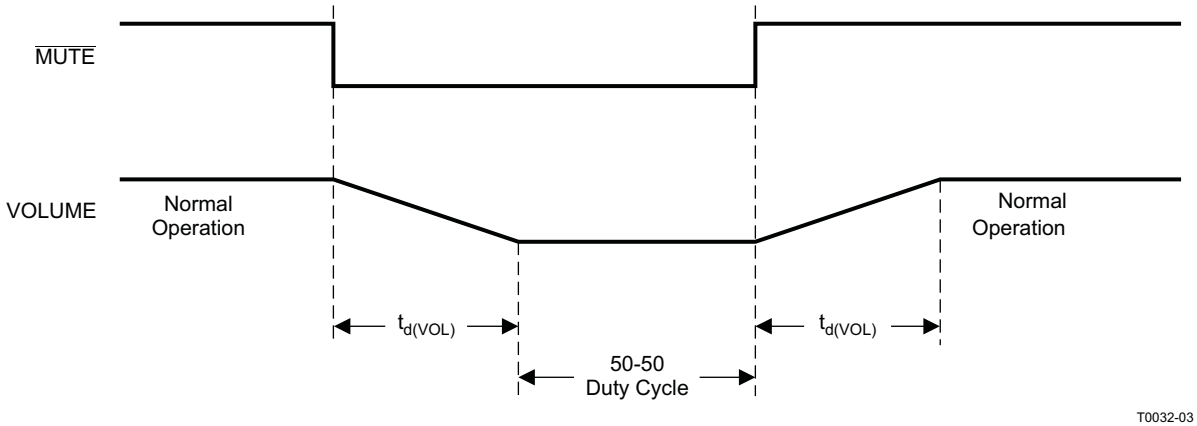



**Figure 7. Mute Timing**

## HEADPHONE SELECT (HPSEL)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{w(MUTE)}$ | Pulse duration, HPSEL active | 350 | None | ns |
| $t_{d(VOL)}$ | Soft volume update time | See (1) | | ms |
| $t_{(SW)}$ | Switch-over time | 0.2 | 1 | ms |

(1) Defined by rate setting. See the Volume Configuration Register section.
Figure 8 and Figure 9 show functionality when bit 4 in HP configuration register is set to DISABLE line output from HP_PWM outputs. If bit 4 is not set, than the HP PWM outputs are not disabled when HPSEL is brought low.

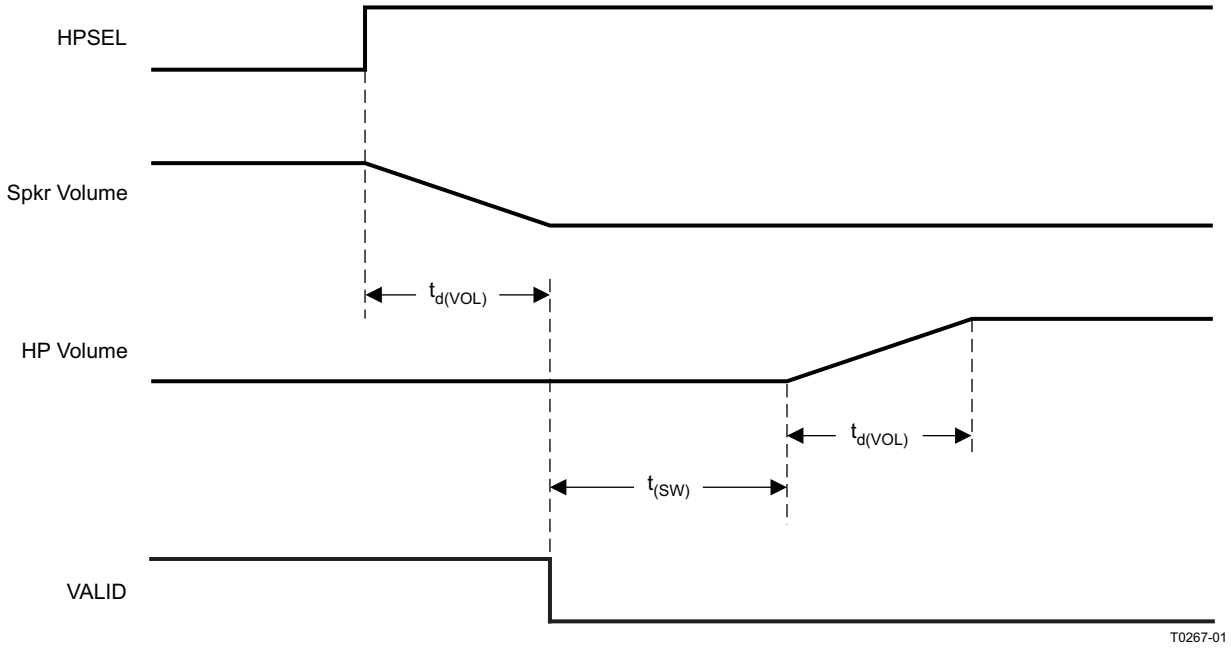



**Figure 8. HPSEL Timing for Headphone Insertion**

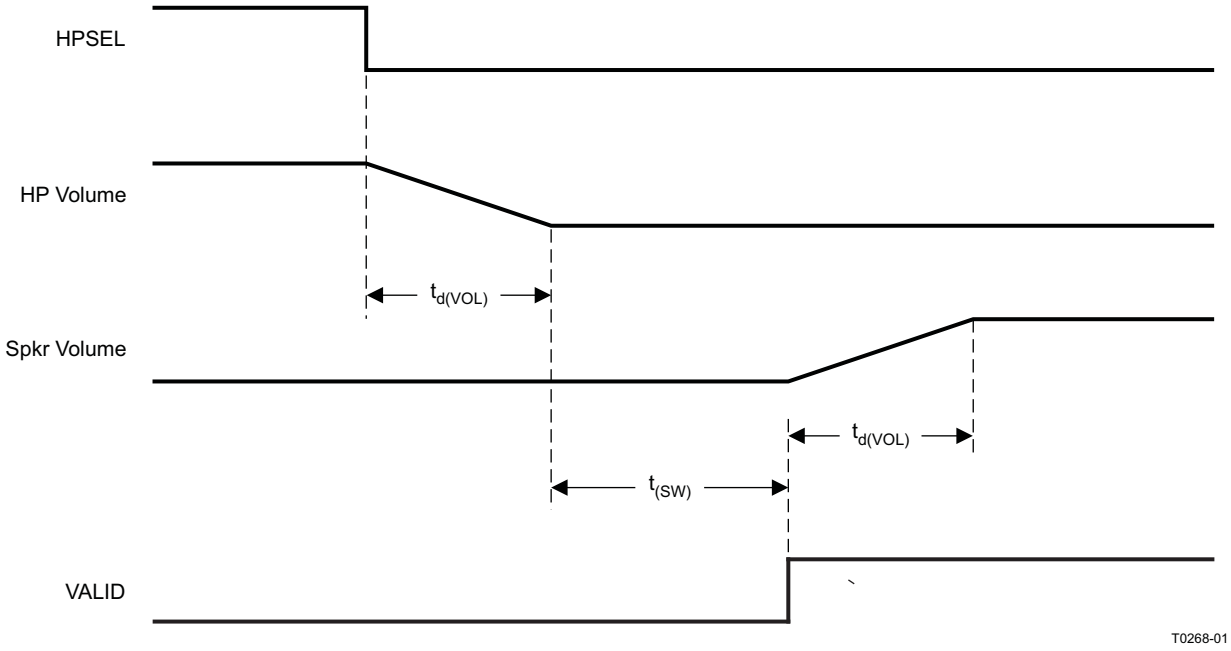



**Figure 9. HPSEL Timing for Headphone Extraction**

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION

**TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY**

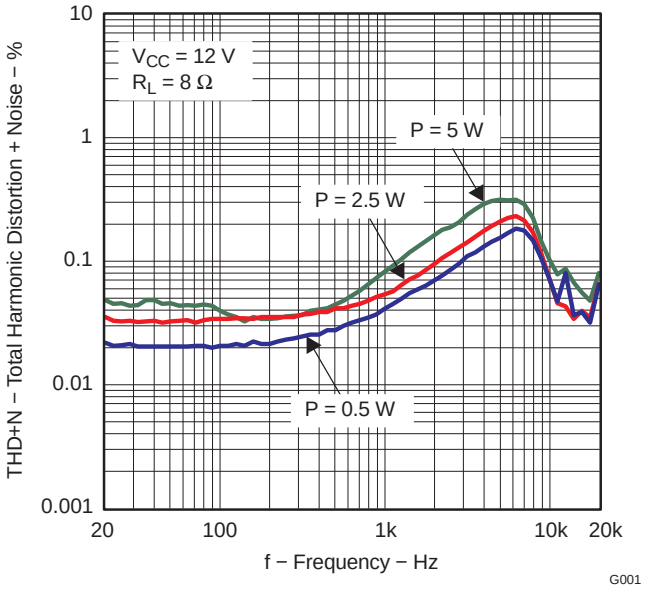



**Figure 10.**

**TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY**

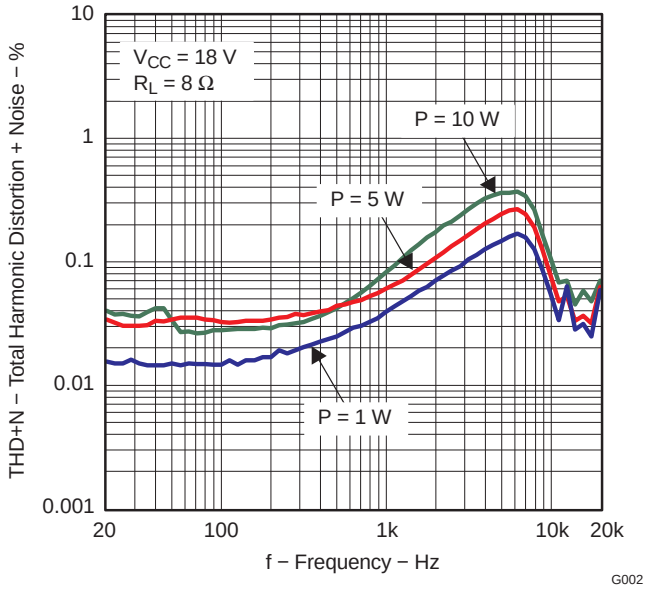



**Figure 11.**

**TOTAL HARMONIC DISTORTION + NOISE (BTL) vs FREQUENCY**

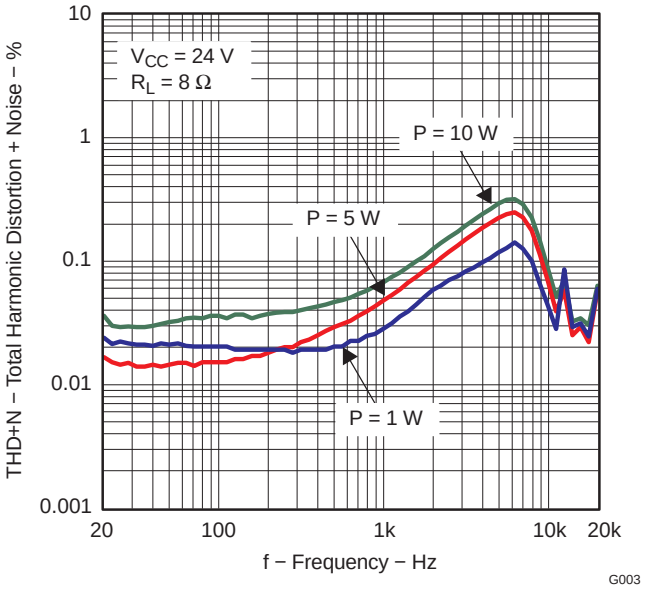



**Figure 12.**

**TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER**

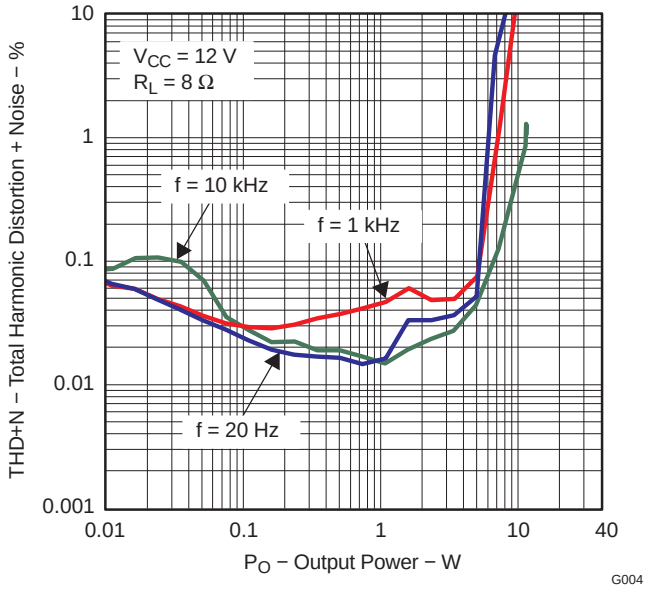



**Figure 13.**

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

**TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER**

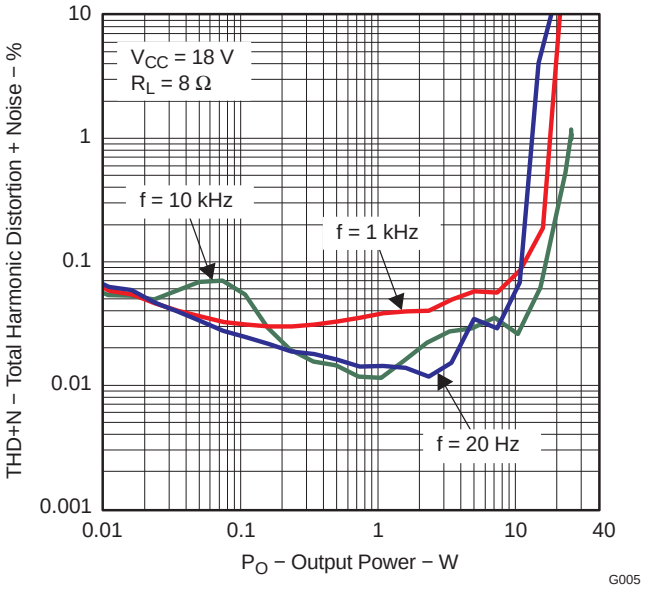



**Figure 14.**

**TOTAL HARMONIC DISTORTION + NOISE (BTL) vs OUTPUT POWER**

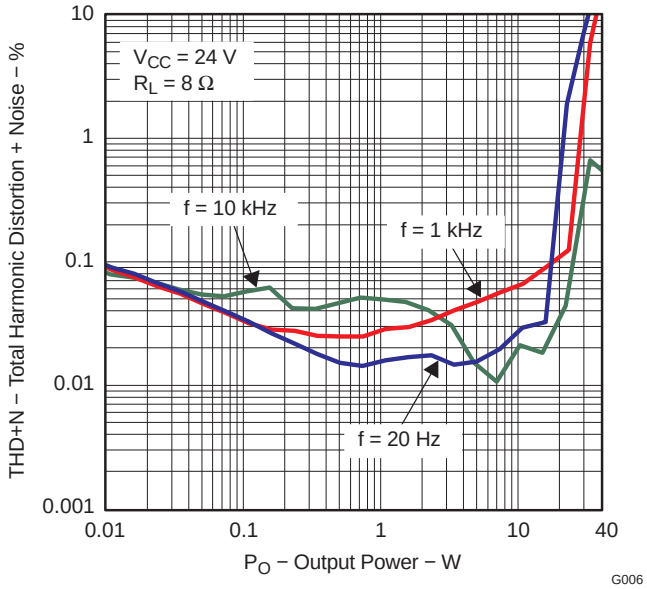



**Figure 15.**

**EFFICIENCY vs OUTPUT POWER**

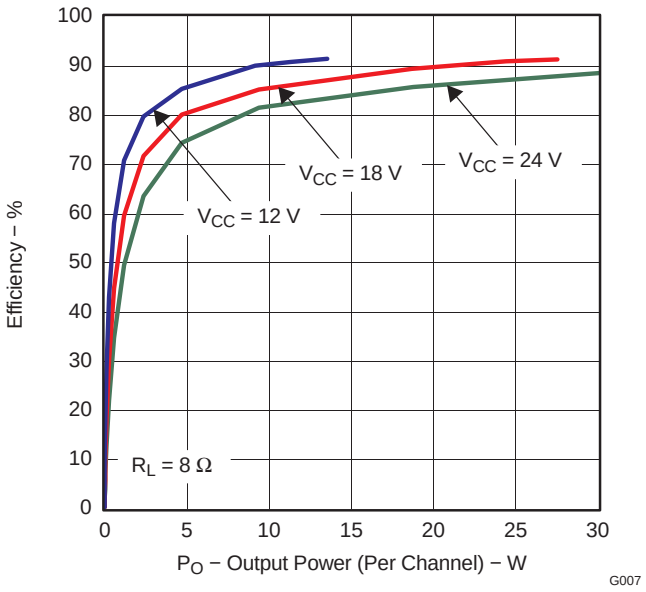



**Figure 16.**

**SUPPLY CURRENT vs TOTAL OUTPUT POWER**

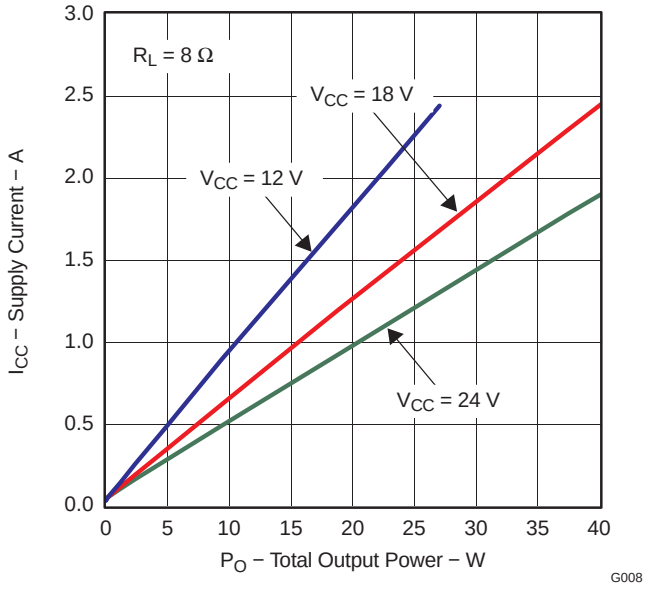



**Figure 17.**

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

**OUTPUT POWER vs SUPPLY VOLTAGE**

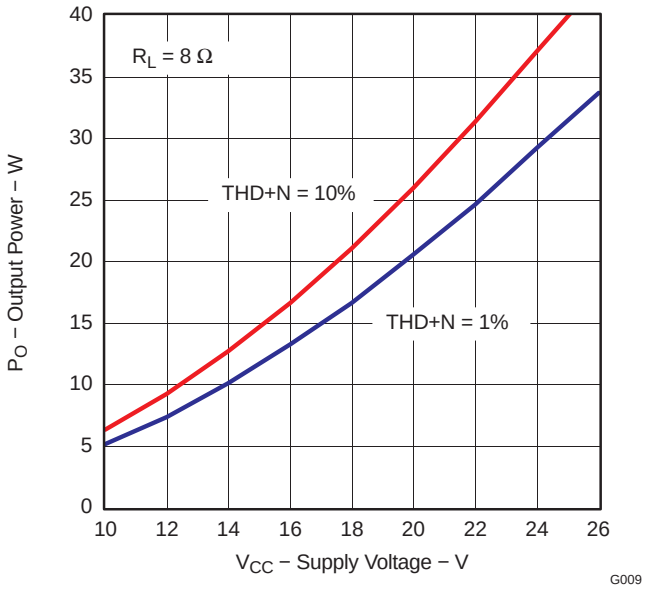



**Figure 18.**

**PSRR vs PVCC**

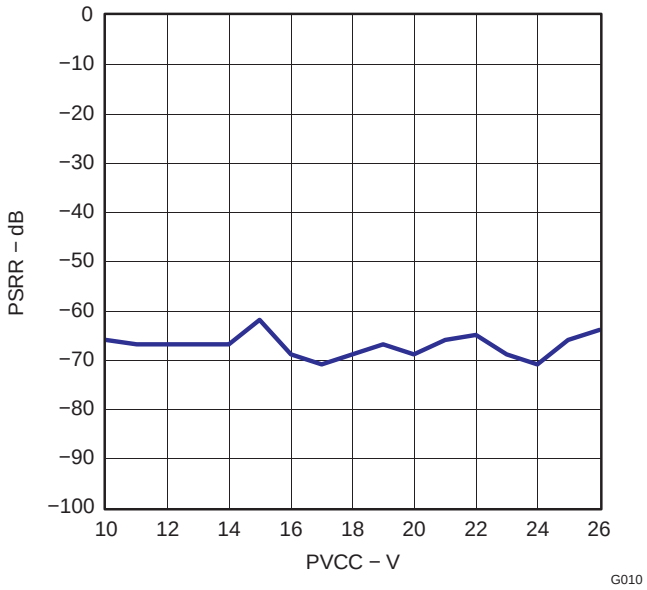



**Figure 19.**

**A-WTD NOISE vs PVCC**

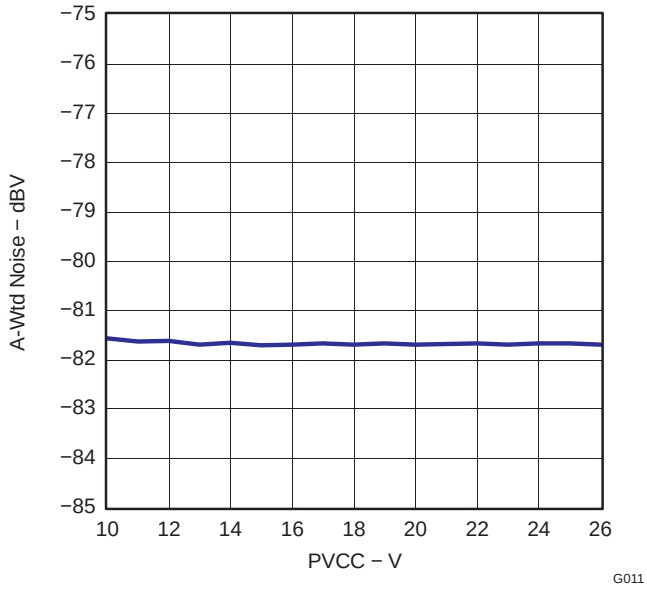



**Figure 20.**

**CROSSTALK vs FREQUENCY**

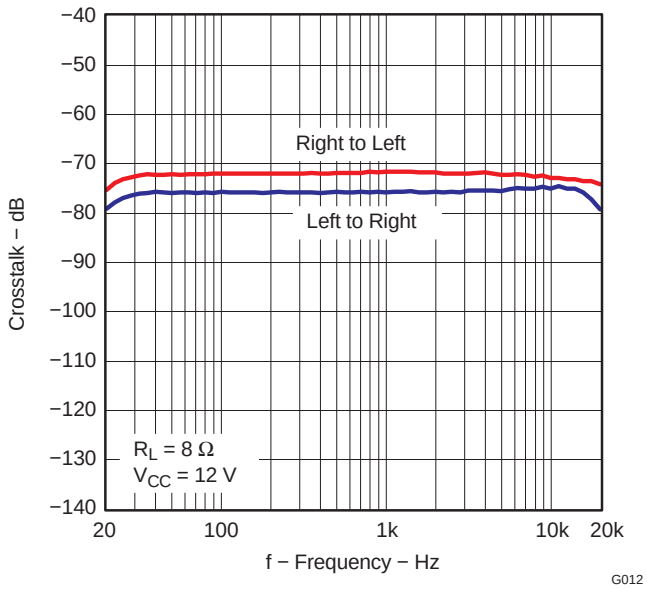



**Figure 21.**

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

**CROSSTALK vs FREQUENCY**

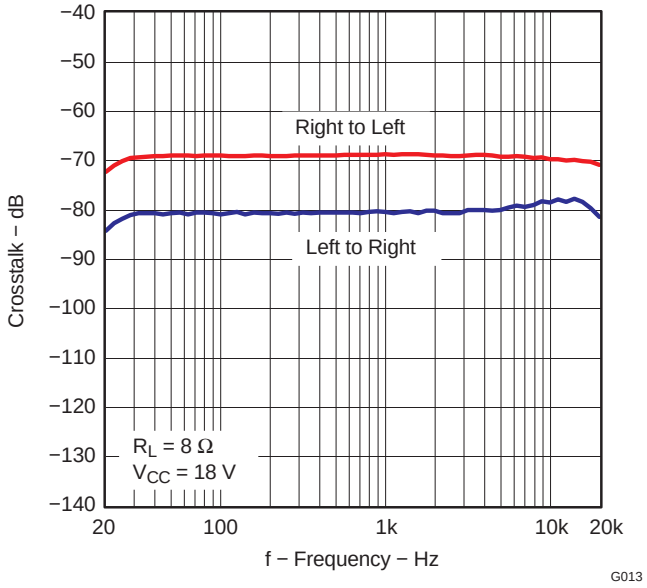



**Figure 22.**

**CROSSTALK vs FREQUENCY**

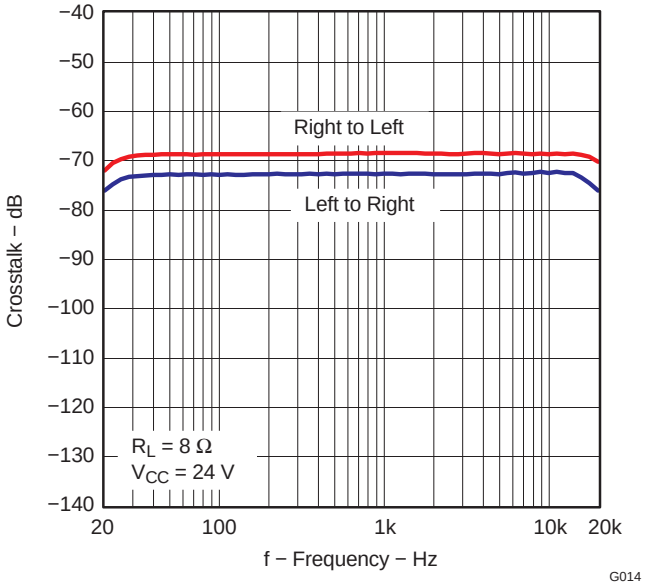



**Figure 23.**

## TYPICAL CHARACTERISTICS, SE CONFIGURATION

**TOTAL HARMONIC DISTORTION + NOISE (SE) vs FREQUENCY**

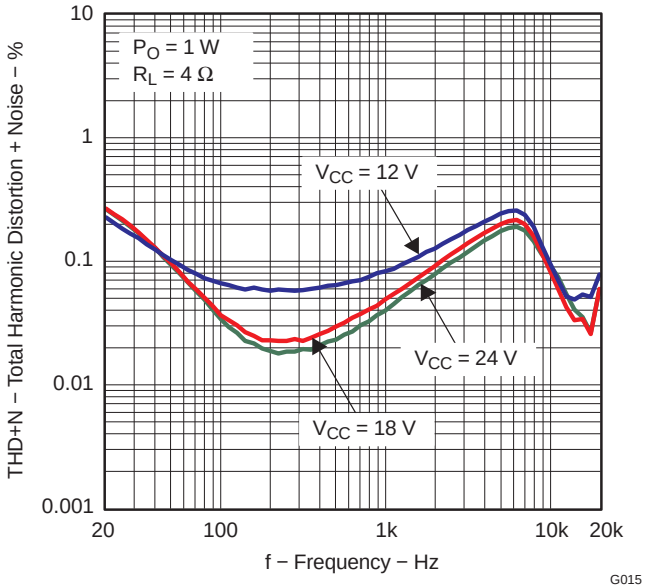



**Figure 24.**

**TOTAL HARMONIC DISTORTION + NOISE (SE) vs OUTPUT POWER**

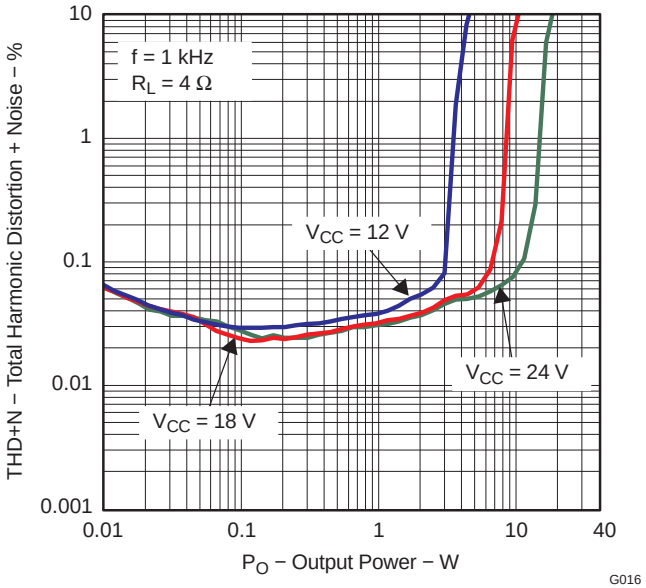



**Figure 25.**

## TYPICAL CHARACTERISTICS, SE CONFIGURATION (continued)

**EFFICIENCY vs OUTPUT POWER**

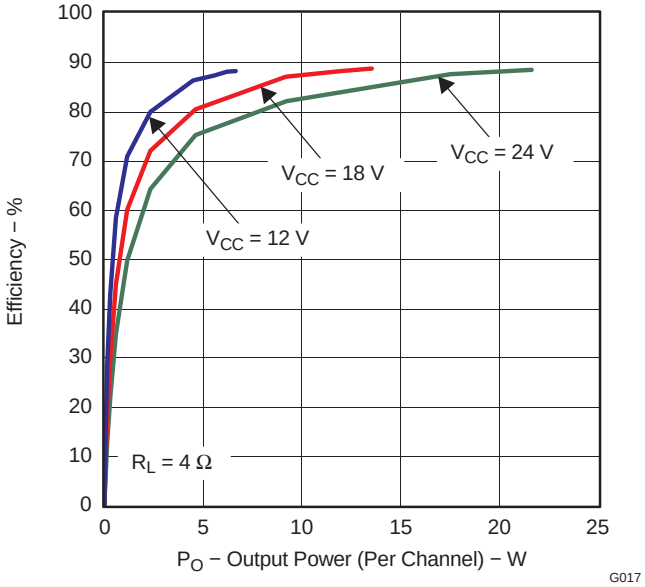



**Figure 26.**

**SUPPLY CURRENT vs TOTAL OUTPUT POWER**

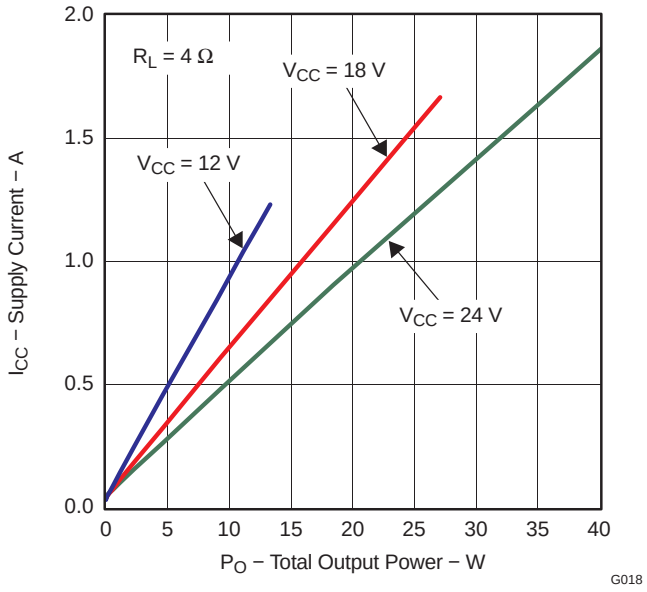



**Figure 27.**

**OUTPUT POWER vs SUPPLY VOLTAGE**

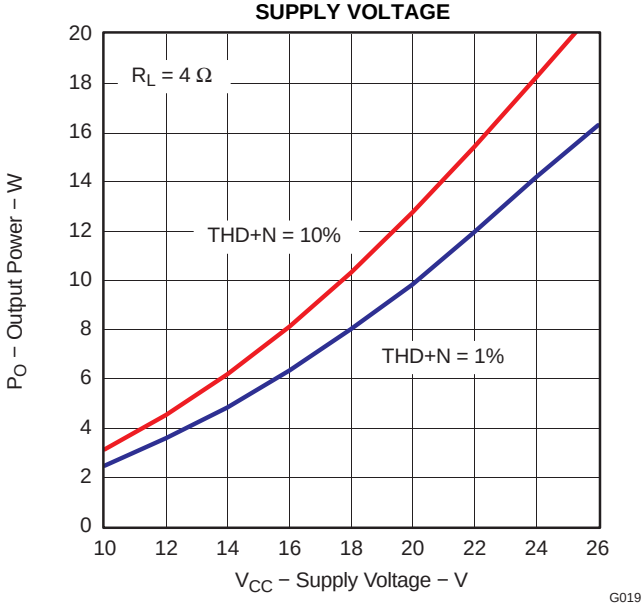



**Figure 28.**

# DETAILED DESCRIPTION

## POWER SUPPLY

The digital portion of the chip requires 3.3 V, and the power stages can work from 10 V to 26 V.

## CLOCK, AUTO DETECTION, AND PLL

The TAS5706 DAP is a slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the clock control register .

The TAS5706 checks to verify that SCLK is a specific value of 32 $f_S$, 48 $f_S$, or 64 $f_S$. The DAP only supports a 1 × $f_S$ LRCLK. The timing relationship of these clocks to SDIN1/2 is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to produce the internal clock.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz or 192 kHz). The automatic sample rate detection can be disabled and the values set via $I^2C$ in the clock control register.

The DAP also supports an AM interference-avoidance mode during which the clock rate is adjusted, in concert with the PWM sample rate converter, to produce a PWM output at 7 × $f_S$, 8 × $f_S$, or 6 × $f_S$.

The sample rate must be set manually during AM interference avoidance and when de-emphasis is enabled.

## SERIAL DATA INTERFACE

Serial data is input on SDIN1/2. The PWM outputs are derived from SDIN1/2. The TAS5706 DAP accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 18-, 20-, or 24-bit data in left-justified, right-justified, and $I^2S$ serial data formats.

### PWM Section

The TAS5706 DAP device uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper that has >100-dB SNR performance from 20 Hz to 20 kHz. The PWM section accepts 24-bit PCM data from the DAP and outputs four PWM audio output channels. TAS5706 PWM section output supports bridge-tied loads.

The PWM section has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual channel de-emphasis filters for 32-, 44.1-, and 48-kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

## $I^2C$ COMPATIBLE SERIAL CONTROL INTERFACE

The TAS5706 DAP has an $I^2C$ serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100-kHz) and high-speed (400-kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

The serial control interface supports both single-byte and multi-byte read and write operations for status registers and the general control registers associated with the PWM.

The $I^2C$ interface supports a special mode which permits $I^2C$ write operations to be broken up into multiple-data write operations that are multiples of 4 data bytes. These are 6-, 10-, 14-, 18-, ... etc., -byte write operations that are composed of a device address, read/write bit, subaddress, and any multiple of 4 bytes of data. This permits the system to write large register values incrementally without blocking other $I^2C$ transactions.

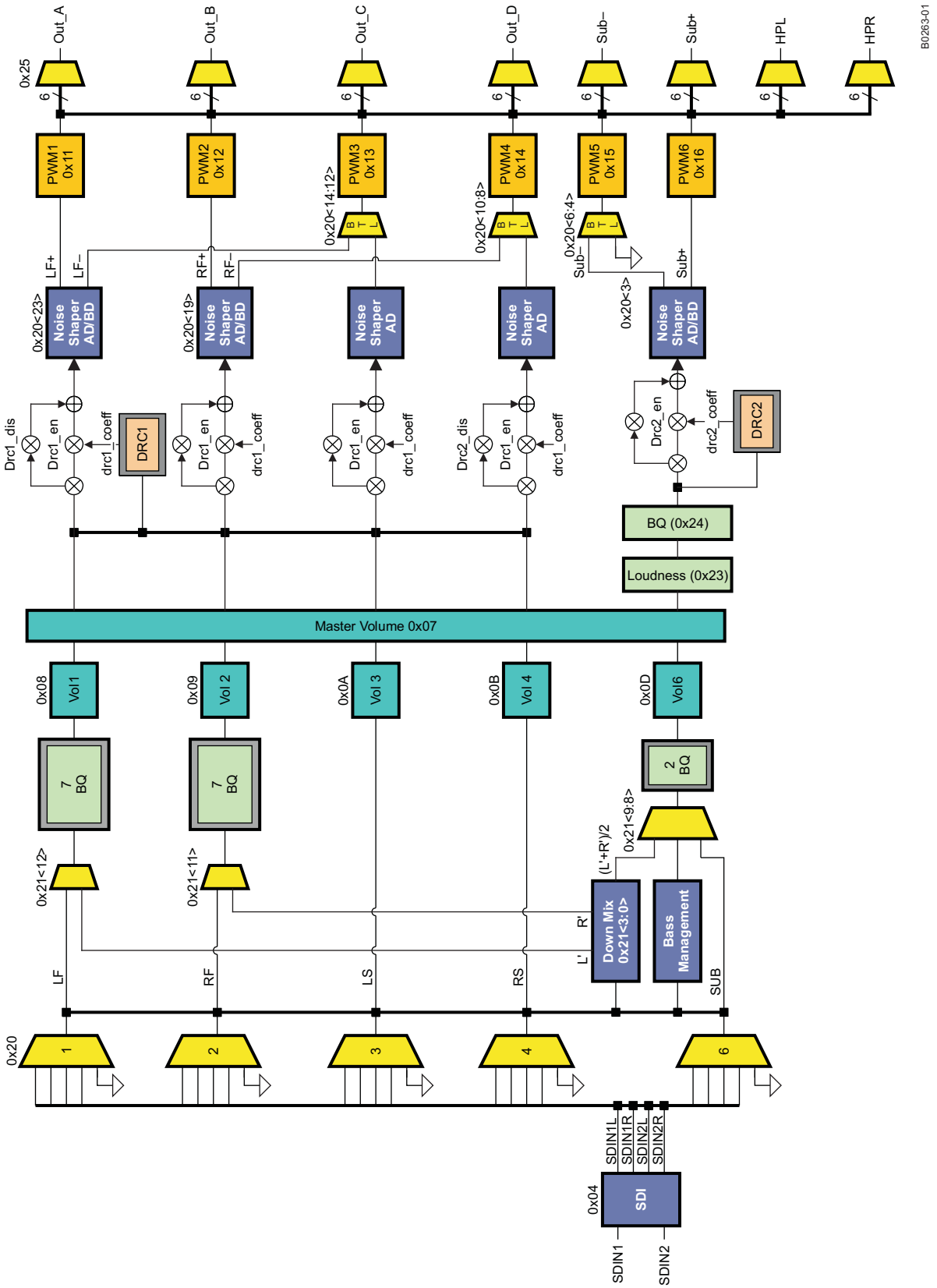
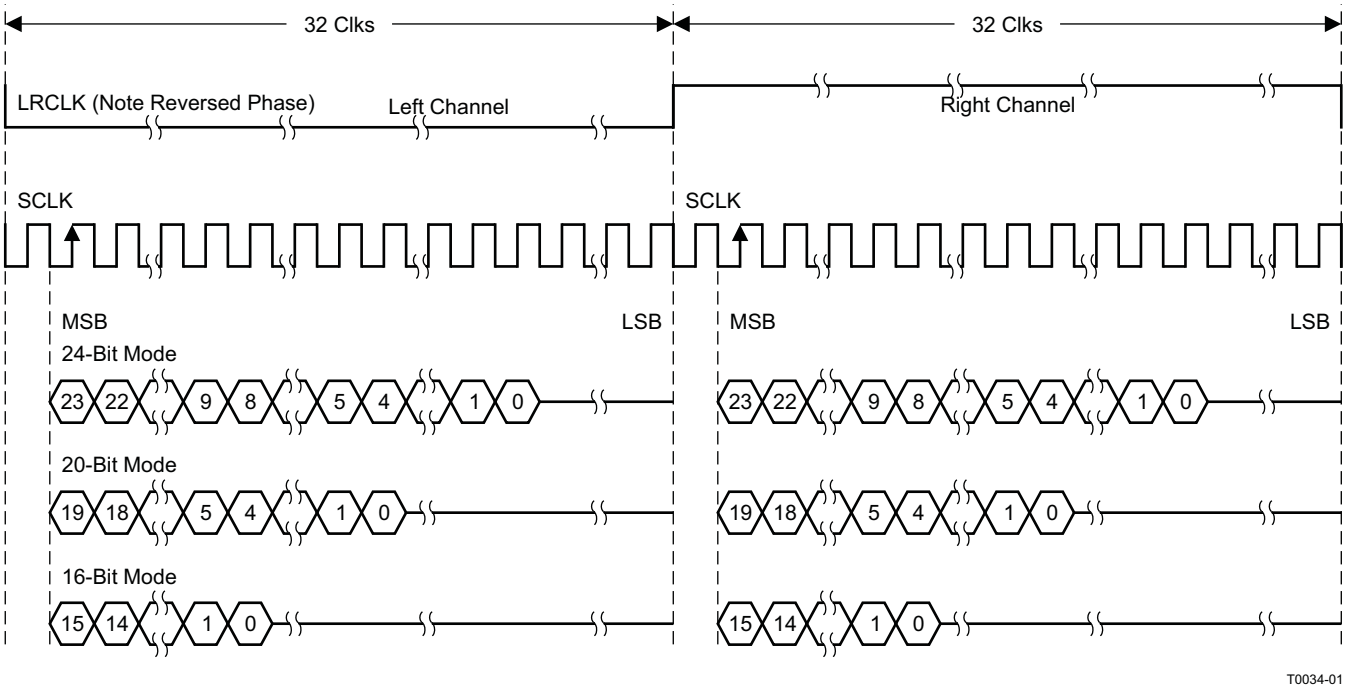



**Figure 29. TAS5706 DAP Data Flow Diagram With I²C Registers**

## I²S Timing

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

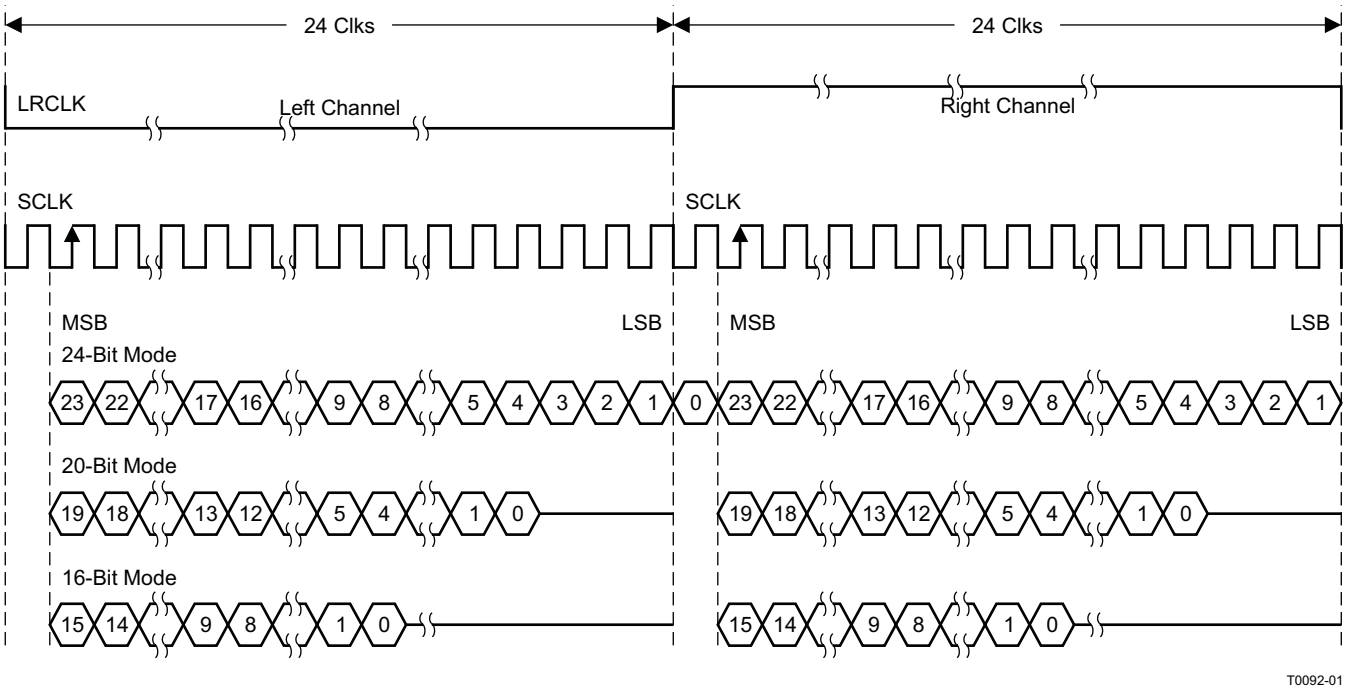
2-Channel I²S (Philips Format) Stereo Input




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 30. I²S 64-$f_S$ Format**

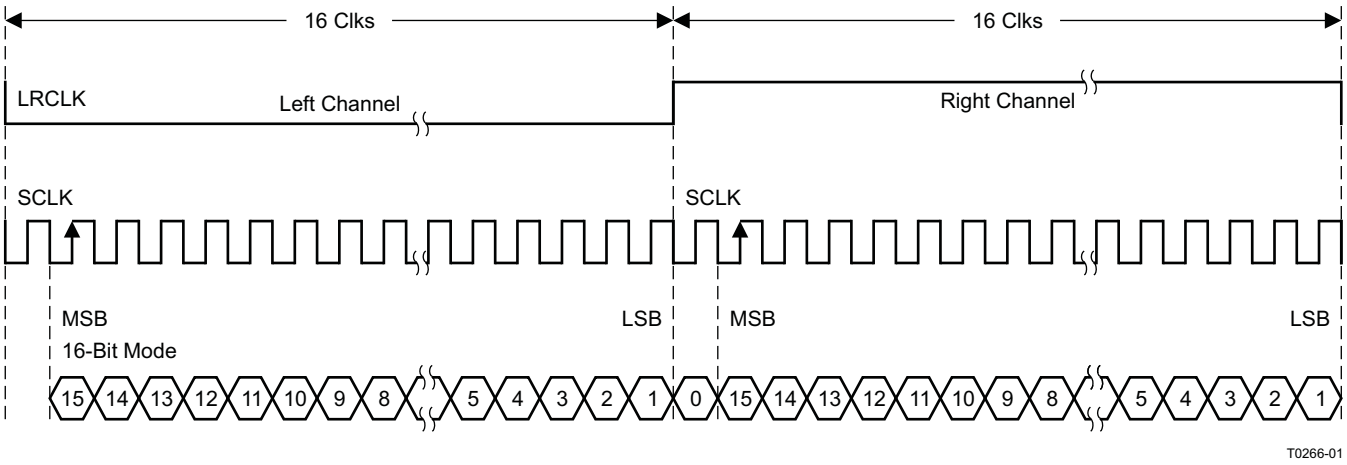
2-Channel I$^2$S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 31. I$^2$S 48-$f_S$ Format**

2-Channel I$^2$S (Philips Format) Stereo Input



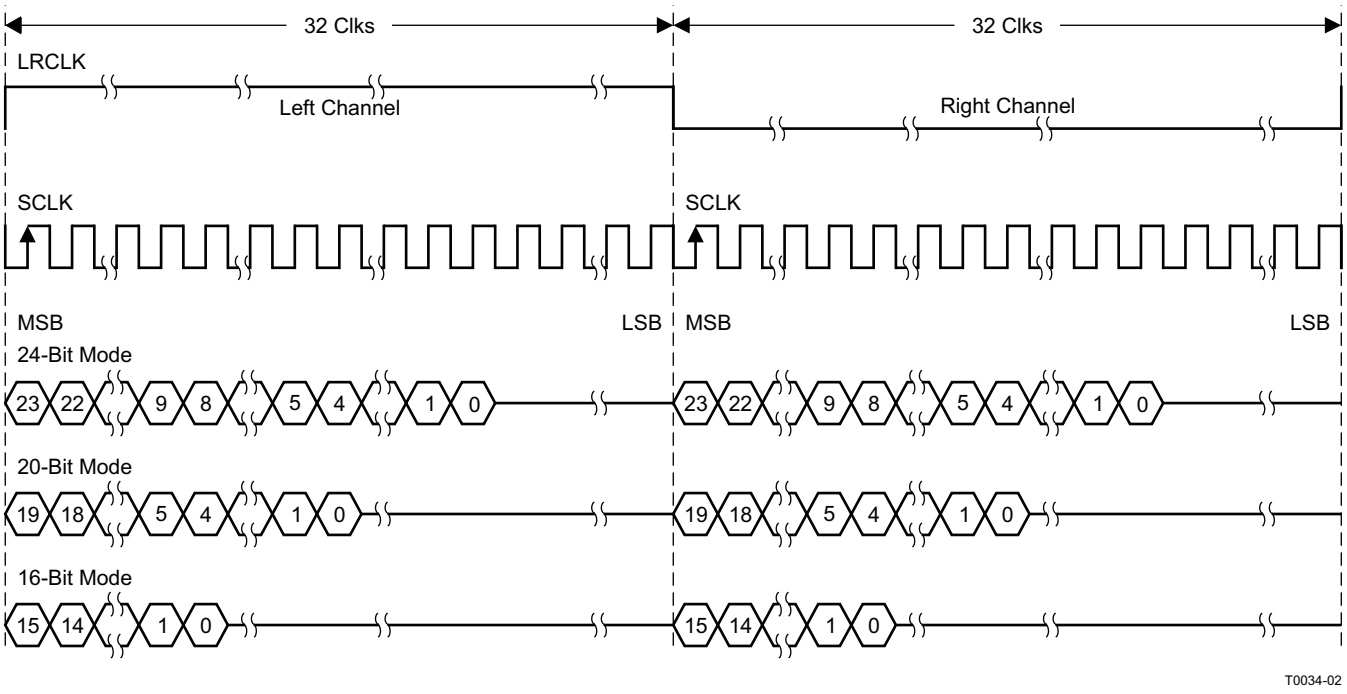

NOTE: All data presented in 2s-complement form with MSB first.

**Figure 32. I$^2$S 32-$f_S$ Format**

## Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

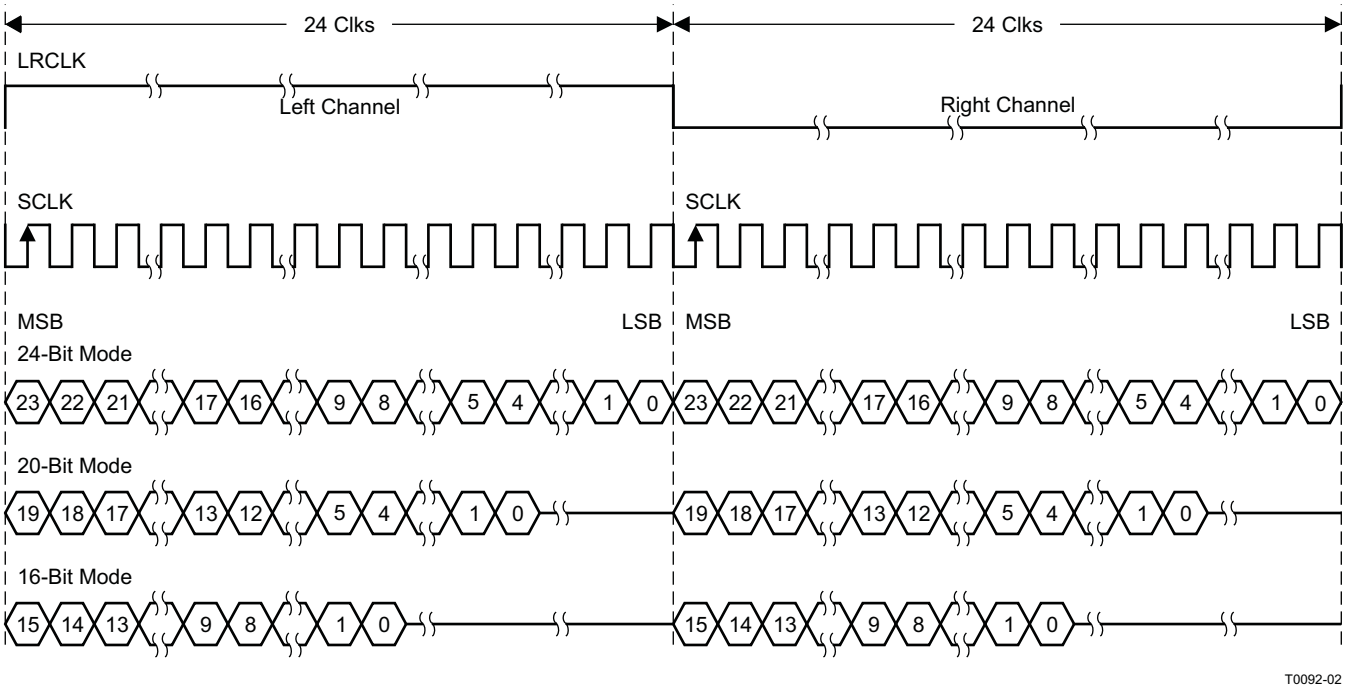
2-Channel Left-Justified Stereo Input




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 33. Left-Justified 64-$f_S$ Format**

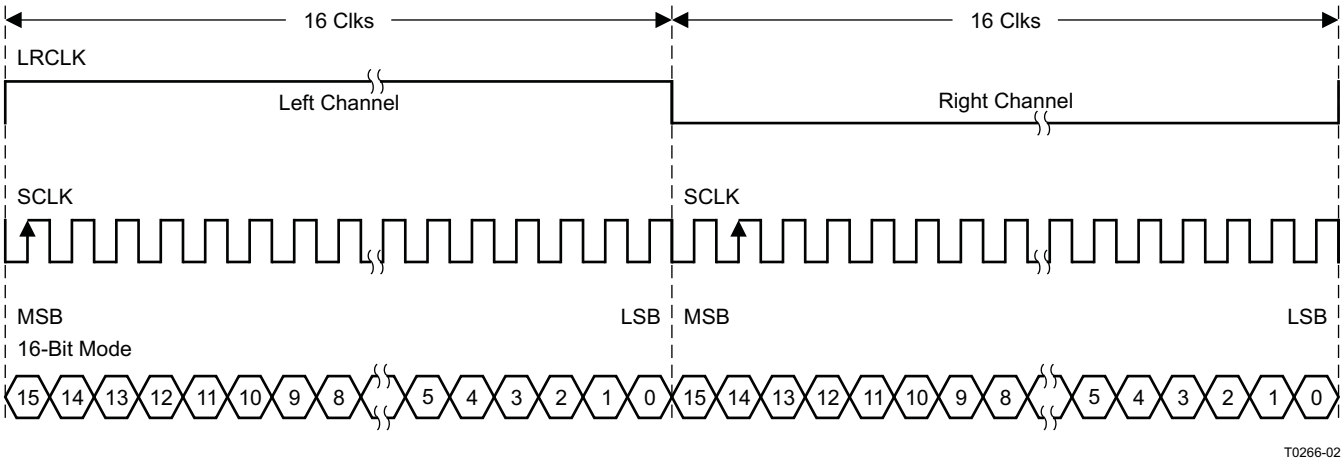
2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 34. Left-Justified 48-$f_S$ Format**

2-Channel Left-Justified Stereo Input




NOTE: All data presented in 2s-complement form with MSB first.

**Figure 35. Left-Justified 32-$f_S$ Format**

## Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

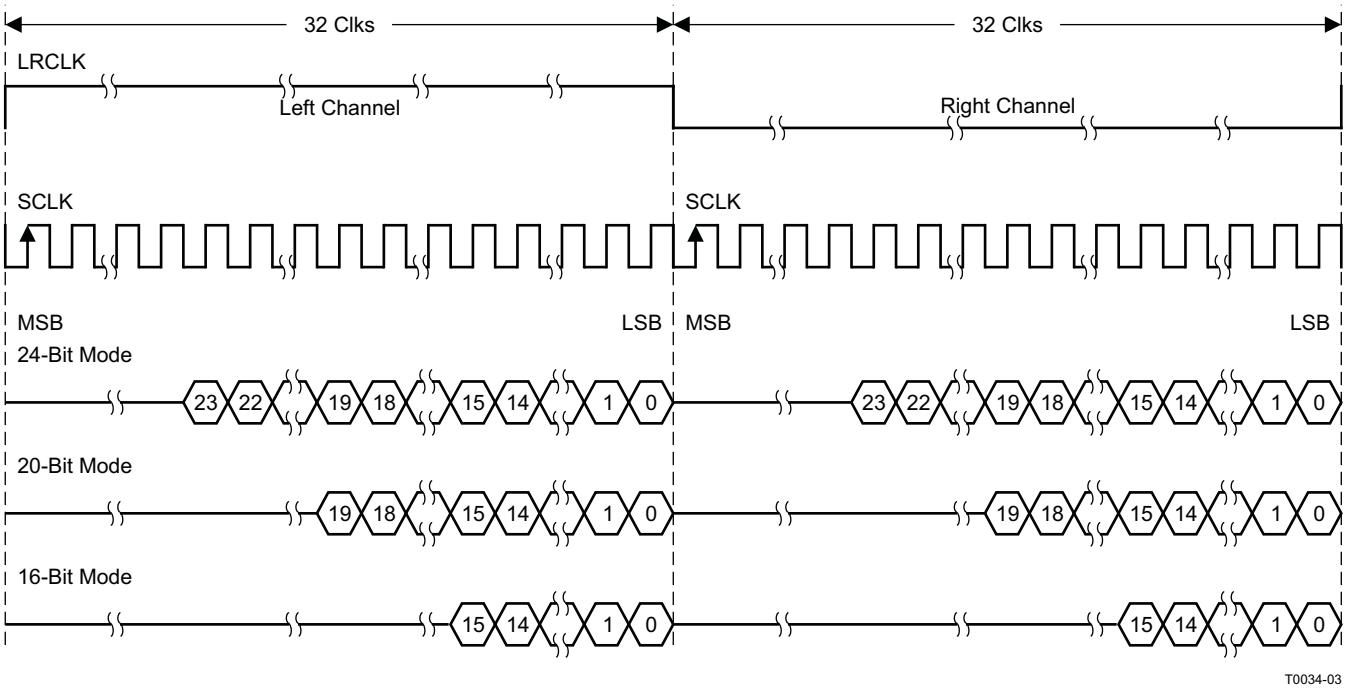



**Figure 36. Right Justified 64-$f_S$ Format**

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

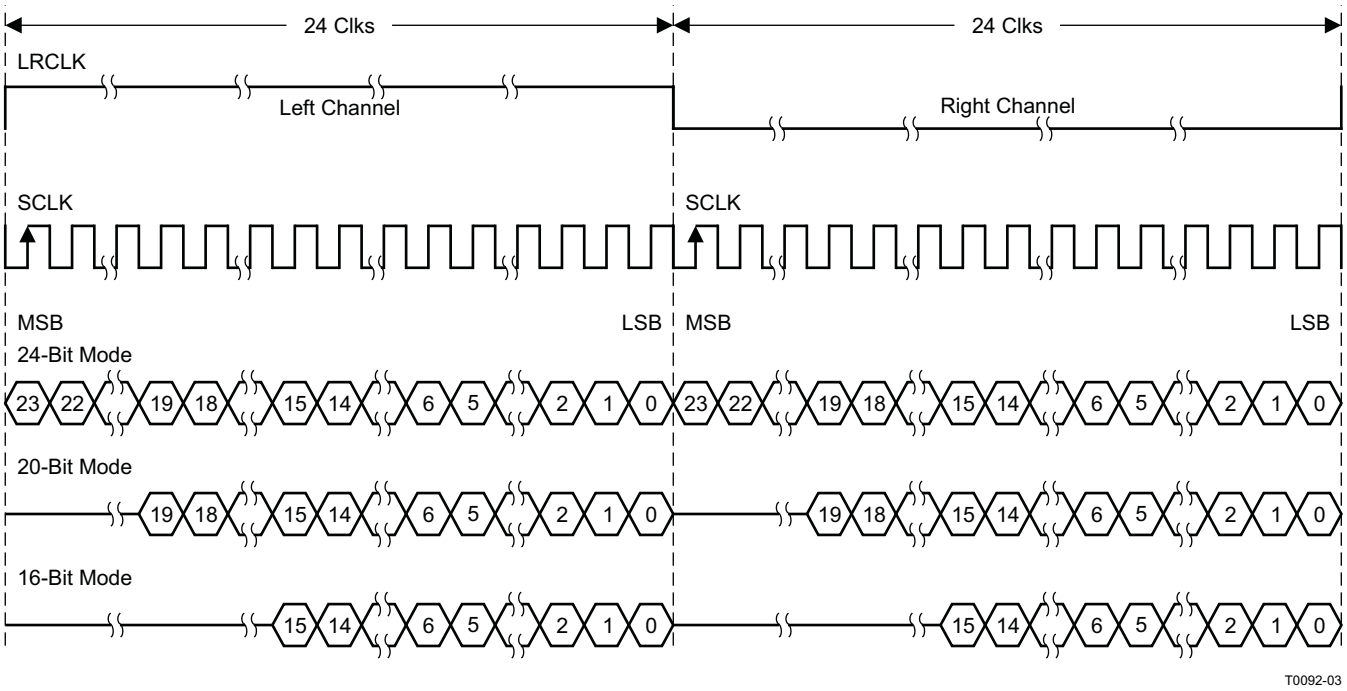



**Figure 37. Right Justified 48-$f_S$ Format**

2-Channel Right-Justified (Sony Format) Stereo Input

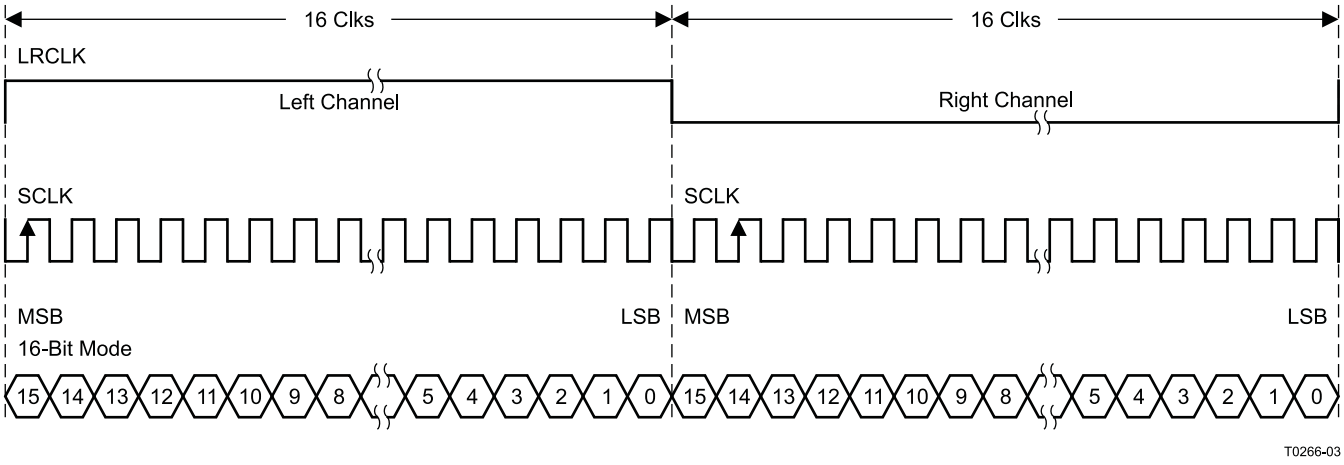



**Figure 38. Right Justified 32-$f_S$ Format**

## I²C SERIAL CONTROL INTERFACE

The TAS5706 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single and multiple byte write and read operations. This is a slave only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

### General I²C Operation

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 39. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5706 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

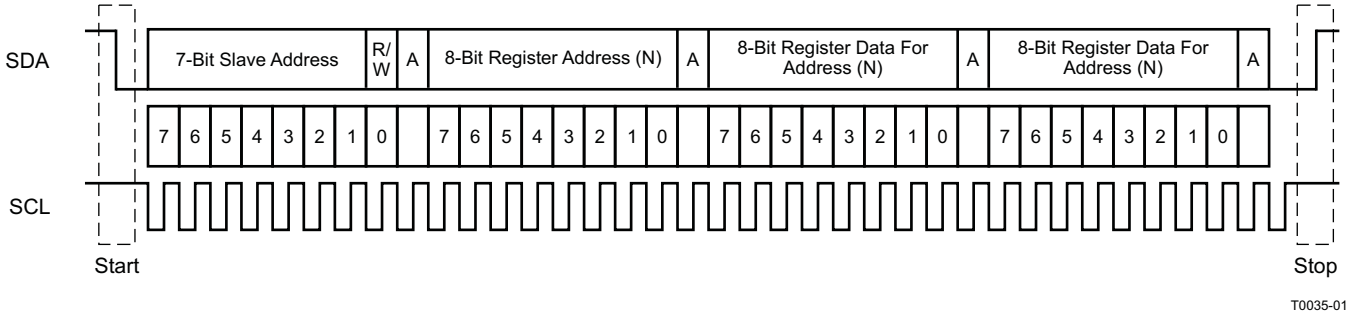



**Figure 39. Typical I²C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 39.

The 7-bit address for TAS5706 is 0011 011 (0x36).

### Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial control interface supports only multiple-byte (4-byte) read/write operations.

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. If a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded. Similarly, if a write command is received for a mixer coefficient, the DAP expects to receive one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random $I^2C$ addressing. The TAS5706 also supports sequential $I^2C$ addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential $I^2C$ write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5706. For $I^2C$ sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

### Single-Byte Write

As shown in Figure 40, a single-byte data write transfer begins with the master device transmitting a start condition followed by the $I^2C$ device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct $I^2C$ device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5706 internal memory address being accessed. After receiving the address byte, the TAS5706 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5706 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

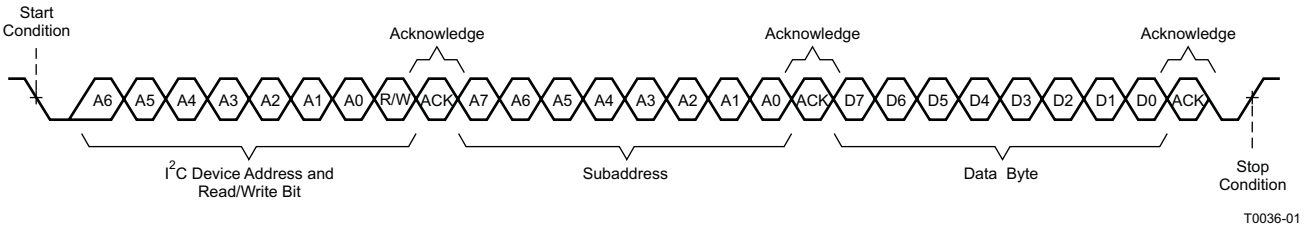



**Figure 40. Single-Byte Write Transfer**

### Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 41. After receiving each data byte, the TAS5706 responds with an acknowledge bit.

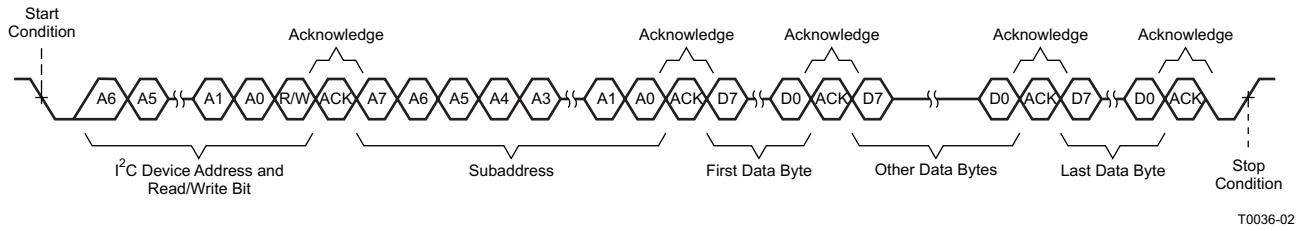



**Figure 41. Multiple-Byte Write Transfer**

### Single-Byte Read

As shown in Figure 42, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5706 address and the read/write bit, TAS5706 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5706 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5706 again responds with an acknowledge bit. Next, the TAS5706 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

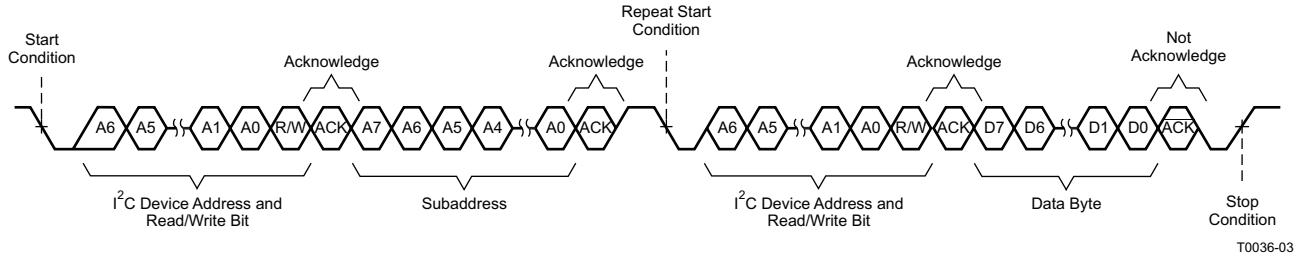



**Figure 42. Single-Byte Read Transfer**

### Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5706 to the master device as shown in Figure 43. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

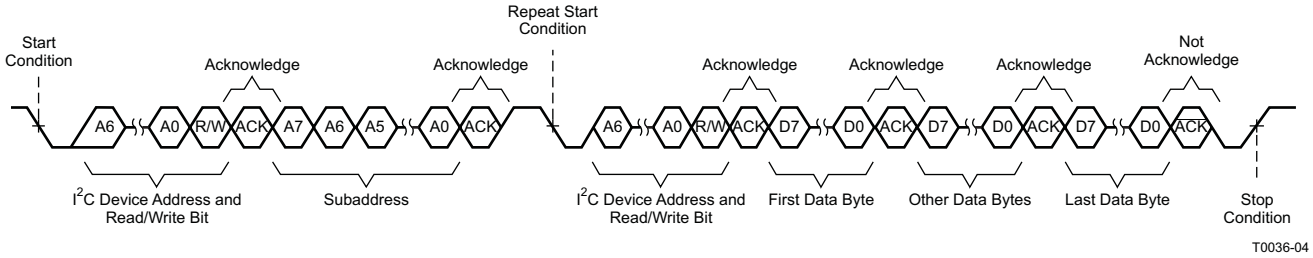
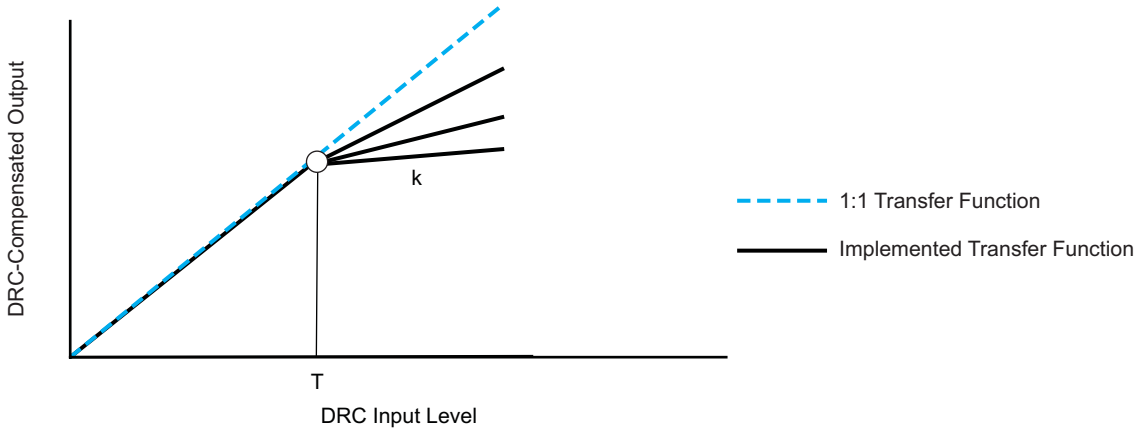



**Figure 43. Multiple Byte Read Transfer**

### Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/right channels and one DRC for the subwoofer channel.

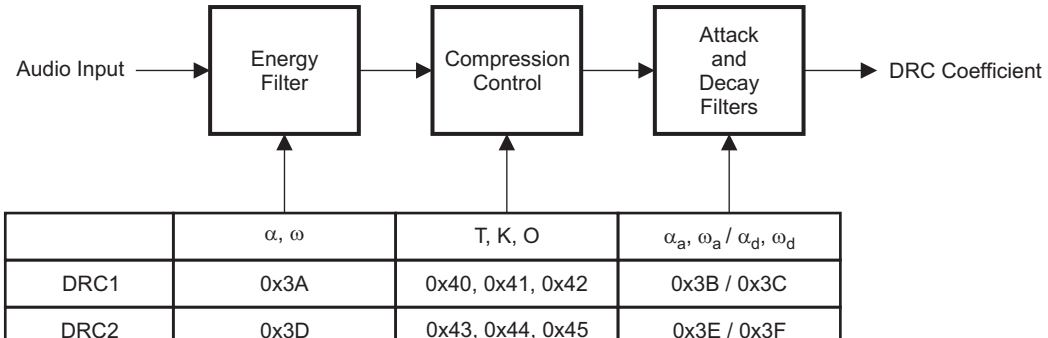
The DRC input/output diagram is shown in Figure 44.



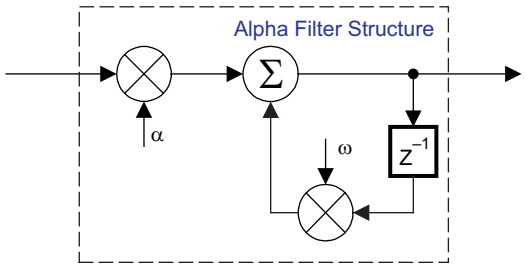

Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- One DRC for left/right and one DRC for subwoofer
- Each DRC has adjustable threshold, offset, and compression levels
- Programmable energy, attack, and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

**Figure 44. Dynamic Range Control**




| | $\alpha$, $\omega$ | T, K, O | $\alpha_a$, $\omega_a$ / $\alpha_d$, $\omega_d$ |
|---|---|---|---|
| DRC1 | 0x3A | 0x40, 0x41, 0x42 | 0x3B / 0x3C |
| DRC2 | 0x3D | 0x43, 0x44, 0x45 | 0x3E / 0x3F |




NOTE:
$\alpha = a$
$\omega = 1 - a$

**Figure 45. DRC Structure**

### Loudness Function

The TAS5706 provides a direct form I biquad for loudness on the subwoofer channel. The first biquad is contained in a gain-compensation circuit that maintains the overall system gain at 1 or less to prevent clipping at loud volume settings. This gain compensation is shown in Figure 46

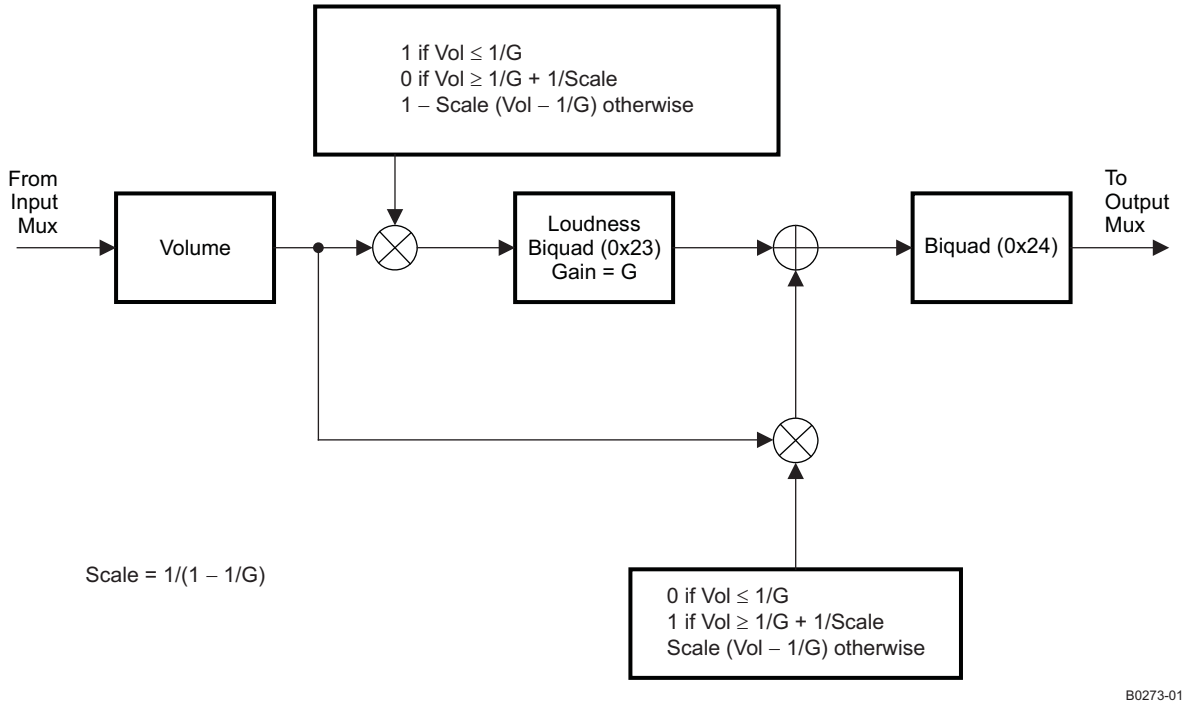



**Figure 46. Biquad Gain Control Structure**

**Table 1. Loudness Table Example for Gain = 4, 1/G = 0.25, Scale = 1.33**

| Volume | 0.125 | 0.25 | 0.375 | 0.5 | 0.625 | 0.75 | 0.875 | 1 | 1.125 | 1.25 | 1.375 | 1.5 | 1.625 | 1.75 | 1.875 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Biquad path | 1 | 1 | 0.833 | 0.666 | 0.5 | 0.333 | 0.166 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Direct path | 0 | 0 | 0.166 | 0.333 | 0.5 | 0.666 | 0.833 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Total gain | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The biquads are implemented in a direct form-I architecture. The direct form-I structure provides a separate delay element and mixer (gain coefficient) for each node in the biquad filter.

The five 26-bit (3.23) coefficients for the biquad are programmable via the $I^2C$ interface.

The following steps are involved in using a loudness biquad with the volume compensation feature:

1. Program the biquad with a loudness filter.
2. Program 0x26 (1/G) and 0x28 (scale).
3. Enable volume compensation in register 0x0E.

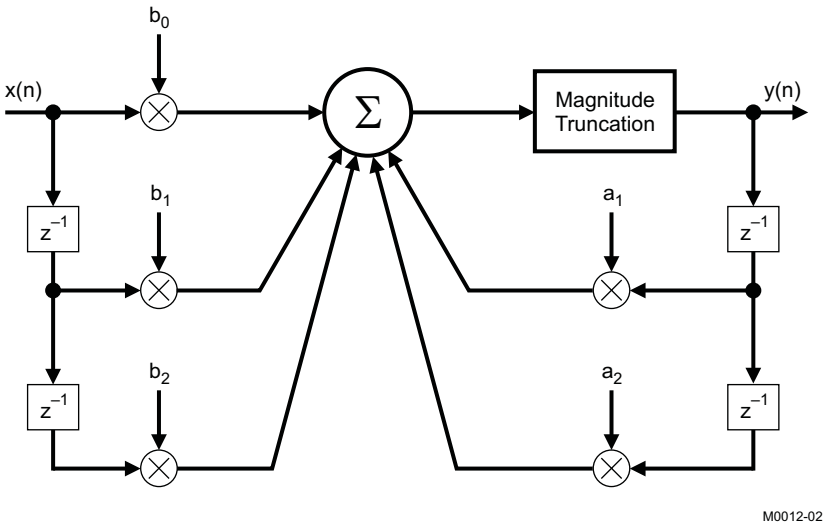



**Figure 47. Biquad Filter**

## BANK SWITCHING

The TAS5706 uses an approach called *bank switching* together with automatic sample-rate detection. All processing features that must be changed for different sample rates are stored internally in the TAS5706. The TAS5706 has three full banks storing information, one for 32 kHz, one for 44.1/48 kHz, and one for all other data rates. Combined with the clock-rate autodetection feature, bank switching allows the TAS5706 to detect automatically a change in the input sample rate and switch to the appropriate bank without any MCU intervention.

The TAS5706 supports three banks of coefficients to be updated during the initialization. One bank is for 32 kHz , a second bank is for 44.1/48 kHz, and a third bank is for all other sample rates. An external controller updates the three banks (see the $I^2C$ register mapping table for bankable locations) during the initialization sequence.

If the autobank switch is enabled (register 0x50, bits 2:0) , then the TAS5706 automatically swaps the coefficients for subsequent sample rate changes, avoiding the need for any external controller intervention for a sample rate change.

By default, bits 2:0 have the value 000; that means the bank switch is disabled. In that state, any update to locations 0x29–0x3F go into the DAP. A write to register 0x50 with bits 2:0 being 001, 010, or 011 brings the system into the coefficient-bank-update state *update bank1*, *update bank2,* or *update bank3*, respectively. Any subsequent write to locations 0x29-0x3F updates the coefficient banks stored outside the DAP. After updating all the three banks, the system controller should issue a write to register 0x50 with bits 2:0 being 100; this changes the system state to automatic bank update. In automatic bank update, the TAS5706 automatically swaps banks based on the sample rate.

In the headphone mode, speaker equalization and DRC are disabled, and they are restored upon returning to the speaker mode.

**Command sequences for initialization can be summarized as follows:**

1. **Enable factory trim for internal oscillator:** Write to register 0x1B with a value 0x00.
2. **Update coefficients:** Coefficients can be loaded into DAP RAM using the manual bank mode.

   OR

   **Use automatic bank mode**.
   (a) Enable bank-1 mode: Write to register 0x50 with 0x01. Load the 32-kHz coefficients. TI ALE can generate coefficients.
   (b) Enable bank-2 mode: Write to register 0x50 with 0x02. Load the 48-kHz coefficients.
   (c) Enable bank-3 mode: Write to register 0x50 with 0x03. Load the other coefficients.
   (d) Enable automatic bank switching by writing to register 0x50 with 0x04.
3. **Bring the system out of all-channel shutdown:** Write 0 to bit 6 of register 0x05.
4. **Issue master volume:** Write to register 0x07 with the volume value (0 db = 0x30).

## APPLICATION INFORMATION

### Recovery From Error

#### *Protection Mechanisms in the TAS5706*

- SCP (short-circuit protection, OCP) protects against shorts across the load, to GND, and to PVCC.
- OTP turns off the device if $T_{die}$ (typical) > 150°C.
- UVP turns off the device if PVCC (typical) < 8.4 V
- OVP turns off the device if PVCC (typical) > 27.5 V

A short-circuit condition can be detected also by an external controller. The SCP error from the external power stage is also fed into TAS5706. The VALID pin goes low in the event of a short circuit. The VALID pin can be monitored by an external μC. The TAS5706 initiates a back-end error sequence by itself to recover from the error, which involves settling VALID low for a programmable amount of time and then retrying to check whether the SCP condition still exists.

- OTP turns on the device back when $T_{die}$(typical) < 135°C.
- UVP turns on the device if PVCC (typical) is > 8.5 V.
- OVP turns on the device if PVCC (typical) is < 27.2 V.

### Interchannel Delay (ICD) Settings

**Table 2. Recommended ICD Settings**

| Mode | Description | ICD1 | ICD2 | ICD3 | ICD4 | ICD5 | ICD6 |
|---|---|---|---|---|---|---|---|
| 2.0 ch BD BTL | 2 BTL channels, internal power stage only, BD mode | A(L+) = 19 (0x4C) | C(R+) = 13 (0x34) | B(L–) = 7 (0x1C) | D(R–) = 25 (0x64) | SM(S–) = –12 (0xD0) | SP(S+) = –28 (0x90) |
| 2.1 ch AD BTL | 2 internal BTL channels, 1 external BTL channel using PBTL TAS5601, AD mode | A(L+) = 23 (0x5C) | C(R+) = 9 (0x24) | B(L–) = 21 (0x54) | D(R–) = 11 (0x2C) | SM(S–) = –23 (0xA4) | SP(S+) = –21 (0xAC) |
| 2.1 ch AD SE | 2 internal SE channels (2 unused), 1 external BTL channel using PBTL TAS5601, AD mode | A(L+) = 15 (0x3C) | B(R–) = –15 (0xC4) | B(0) = 0 (0x00) | D(0) = 0 (0x00) | SM(S–) = –30 (0x88) | SP(S+) = –32 (0x80) |
| 2.1 ch BD BTL | 2 internal BTL channels, 1 external BTL channel using PBTL TAS5601, BD mode | A(L+) = 19 (0x4C) | C(R+) = 13 (0x34) | B(L–) = 7 (0x1C) | D(R–) = 25 (0x64 ) | SM(S–) = –12 (0xD0) | SP(S+) = –28 (0x90) |
| 3.0 ch AD 2SE + 1 BTL | 2 internal SE channels + 1 internal BTL channel, AD mode | A(L+) = 15 (0x3C) | B(R–) = –16 (0xC0) | SM(0) = 0 (0x00) | SP(0) = 0 (0x00) | D(S–) = 0 (0x00) | C(S+) = 2 (0x08) |
| 4.0 ch AD SE | 4 internal SE channels | A(L1+) = 8 (=0x20) | B(R1–) = –24 (0xA0) | C(L2+) = –8 (0xE0) | D(R2–) = 24 (0x60) | SM(0) = 1 (0x04) | SP(0) = –1 (0xFC) |
| 4.1 ch AD SE | 4 internal SE channels + 1 external BTL channel, using PBTL TAS5601, AD mode. | A(L1+) = 8 (0x20) | B(R1–) = –24 (0xA0) | C(L2+) = –8 (xE0) | D(R2–)= 24 (0x60) | SM(S–) = 1 (0x04) | SP(S+) = –1 (0xFC) |

### Calculation of Output Signal Level of TAS5706 Feedback Power Stage (Gain Is independent of PVCC)

The gain of the TAS5706 is the total digital gain of the controller multiplied by the gain of the power stage.

For a half-bridge channel of the TAS5706 power stage, the gain is simply:

Power stage gain = 13 × $V_{RMS}$ / Modulation Level

Modulation level = fraction of full-scale modulation of the PWM signal at the input of the power stage.

$V_{RMS}$ = Audio voltage level at the output of the power stage = 13 × Modulation Level

For the TAS5706 controller, the gain is the programmed digital gain multiplied by a scaling factor, called the *maximum modulation level*. The maximum modulation level is derived from the modulation limit programmed in the controller, which limits duty cycle to a set number of percent above 0% and below 100%. Setting the modulation limit to 97.7% (default) limits the duty cycle between 2.3% and 97.7%.

Controller gain = digital gain × maximum modulation level × (modulation level/digital FFS)

Digital FFS = digital input fraction of full scale

Modulation limit = 97.7%

Maximum modulation level = 2 × modulation limit – 1 = 0.954

The output signal level of the TAS5706 can now be calculated.

$V_{RMS}$ = digital FFS × digital gain × maximum modulation level × 13

With the modulation limit set at the default level of 97.7%, this becomes:

| | |
|---|---|
| $V_{RMS}$ = digital FFS × digital gain × 12.4 | (Single-ended) |
| $V_{RMS}$ = digital FFS × digital gain × 24.8 | (BTL) |

Example: Input = –20 dbFS; volume = 0 dB; biquads = ALL PASS; modulation index = 97.7%; mode = BTL

Output $V_{RMS}$ = 24.8 × 0.1 × 1 = 2.48 V

## I²C SERIAL CONTROL COMMAND CHARACTERISTICS

The DAP has two groups of I²C commands. One set is commands that are designed specifically to be operated while audio is streaming and that have built-in mechanisms to prevent noise, clicks, and pops. The other set does not have this built-in protection.

**Commands that are designed to be adjusted while audio is streaming:**

- Master volume
- Master mute
- Individual channel volume
- Individual channel mute

**Commands that are normally issued as part of initialization:**

- Serial data interface format
- De-emphasis
- Sample-rate conversion
- Input multiplexer
- Output multiplexer
- Biquads
- Down mix
- Channel delay
- Enable/disable dc blocking
- Hard/soft unmute from clock error
- Enable/disable headphone outputs

**Start-up sequence for correct device operation**

This sequence must be followed to ensure proper operation.

1. Hold ALL logic inputs low. Power up AVDD/DVDD and wait for the inputs to settle in the allowed range. AVDD and DVDD must be ramped up together. The voltage difference between AVDD and DVDD during the ramp must be restricted to no more than 0.4 V.
2. Drive $\overline{\text{PDN}}$ = 1, $\overline{\text{MUTE}}$ = 1, and drive other logic inputs to the desired state.
3. Provide a stable MCLK, LRCLK, and SCLK (clock errors must be avoided during the initialization sequence) .
4. After completing step 3, wait 100 μs, then drive $\overline{\text{RESET}}$ = 1, and wait 13.5 ms after $\overline{\text{RESET}}$ goes high.
5. Trim the internal oscillator (write 0x00 to register 0x1B).
6. Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 μs after AVDD/DVDD reaches 3 V. Then wait at least another 10 μs.
7. Wait 50 ms while the part acquires lock.
8. Configure the DAP via I²C, e.g.:
   - Downmix control (0x21)
   - Biquads (0x23–0x24 and 0x29–0x38)
   - DRC parameters and controls (0x3A–0x46)
   - Bank select (0x50)

   **NOTE: User may not issue any I²C reads or writes to the above registers after this step is complete.**
9. Configure remaining I²C registers, e.g.:
   - Shutdown group
   - De-emphasis
   - Input multiplexers
   - Output multiplexers
   - Channel delays
   - DC blocking
   - Hard/soft unmute from clock error
   - Serial data interface format

– Clock register (manual clock mode only)

**NOTE: The BKND_ERR register (0x1C) can only be written once with a value that is not reserved (00 and 01 are reserved values).**

10. Exit all-channel shutdown (write 0 to bit 6 of register 0x05).
11. This completes the initialization sequence. From this step on, no further constraints are imposed on $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, and clocks.
12. During normal operation the user may do the following:
    (a) Write to the master or individual-channel volume registers.
    (b) Write to the soft-mute register.
    (c) Write to the clock and serial data interface format registers (in manual clock mode only).
    (d) Write to bit 6 of register 0x05 to enter/exit all-channel shutdown. No other bits of register 0x05 may be altered. After issuing the all-channel shutdown command, no further $I^2C$ transactions that address this device are allowed for a period of at least: 1 ms + 1.3 × (period specified in start/stop register 0x1A) .
    (e) $\overline{\text{PDN}}$ may be asserted (low) at any time. Once $\overline{\text{PDN}}$ is asserted, no $I^2C$ transactions that address this device may be issued until $\overline{\text{PDN}}$ has been deasserted and the part has returned to active mode.

**NOTE: When the device is in a powered-down state (initiated via $\overline{\text{PDN}}$), the part is not reset if $\overline{\text{RESET}}$ is asserted.**

**NOTE: Once $\overline{\text{RESET}}$ is asserted, and as long as the part is in a reset state, the part does not power down if $\overline{\text{PDN}}$ is asserted. For powering the part down, a negative edge on $\overline{\text{PDN}}$ must be issued when $\overline{\text{RESET}}$ is high and the part is not in a reset state.**

**NOTE: No registers besides those explicitly listed in Steps a.–d. should be altered during normal operation (i.e., after exiting all-channel shutdown).**

**NOTE: No registers should be read during normal operation (i.e., after exiting all-channel shutdown) .**

13. To reconfigure registers:
    (a) Return to all-channel shutdown (observe the shutdown wait time as specified in Step 11.d.).
    (b) Drive $\overline{\text{PDN}}$ = 1, and hold $\overline{\text{MUTE}}$ stable.
    (c) Provide a stable MCLK, LRCLK, and SCLK.
    (d) Repeat configuration starting from step (6).

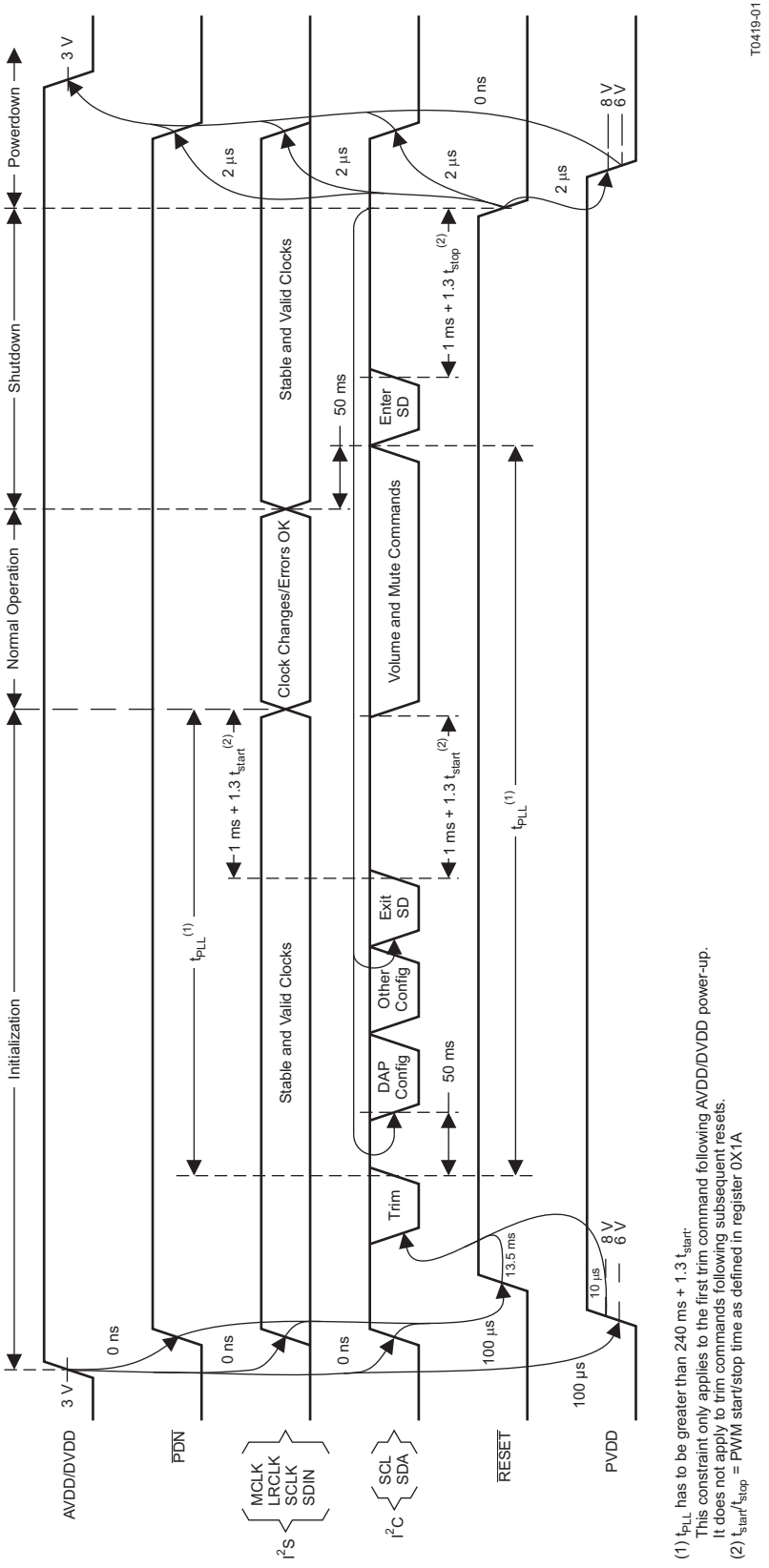



**Figure 48. Start-Up Sequence**

**Table 3. Serial Control Interface Register Summary (1)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| | | | A u indicates unused bits. | |
| 0x00 | Clock control register | 1 | Description shown in subsequent section | 0x6C |
| 0x01 | Device ID register | 1 | Description shown in subsequent section | 0x28 |
| 0x02 | Error status register | 1 | Description shown in subsequent section | 0x00 |
| 0x03 | System control register 1 | 1 | Description shown in subsequent section | 0xA0 |
| 0x04 | Serial data interface register | 1 | Description shown in subsequent section | 0x05 |
| 0x05 | System control register 2 | 1 | Description shown in subsequent section | 0x40 |
| 0x06 | Soft mute register | 1 | Description shown in subsequent section | 0x00 |
| 0x07 | Master volume | 1 | Description shown in subsequent section | 0xFF (mute) |
| 0x08 | Channel 1 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x09 | Channel 2 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0A | Channel 3 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0B | Channel 4 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0C | HP volume | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0D | Channel 6 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0E | Volume configuration register | 1 | Description shown in subsequent section | 0x91 |
| 0x0F | | 1 | Reserved (2) | |
| 0x10 | Modulation limit register | 1 | Description shown in subsequent section | 0x02 |
| 0x11 | IC delay channel 1 | 1 | Description shown in subsequent section | 0x4C |
| 0x12 | IC delay channel 2 | 1 | Description shown in subsequent section | 0x34 |
| 0x13 | IC delay channel 3 | 1 | Description shown in subsequent section | 0x1C |
| 0x14 | IC delay channel 4 | 1 | Description shown in subsequent section | 0x64 |
| 0x15 | IC delay channel 5 | 1 | Description shown in subsequent section | 0xB0 |
| 0x16 | IC delay channel 6 | 1 | Description shown in subsequent section | 0x90 |
| 0x17 | Offset register | 1 | Reserved | 0x00 |
| 0x18 | | 1 | Reserved (2) | |
| 0x19 | PWM shutdown group register | 1 | | 0x30 |
| 0x1A | Start/stop period register | 1 | | 0x0A |
| 0x1B | Oscillator trim register | 1 | | 0x82 |
| 0x1C | BKND_ERR register | 1 | | 0x02 |
| 0x1D–0x1F | | | Reserved (2) | |
| 0x20 | Input MUX register | 4 | Description shown in subsequent section | 0x0089 777A |
| 0x21 | Downmix input MUX register | 4 | Description shown in subsequent section | 0x0000 4203 |
| 0x22 | AM tuned frequency | 4 | Description shown in subsequent section | 0x0000 0000 |
| 0x23 | ch6_bq[2] (Loudness BQ) | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

(1) Biquad definition is given in Figure 47.
(2) Reserved registers should not be accessed.

**Table 3. Serial Control Interface Register Summary [1] (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x24 | ch6_bq[3] (post volume BQ) | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x25 | PWM MUX register | | Description shown in subsequent section | 0x0102 1345 |
| 0x26 | 1/G register | 4 | u[31:26], x[25:0] | 0x0080 0000 |
| 0x27 | | 1 | Reserved [2] | |
| 0x28 | Scale register | 4 | u[31:26], x[25:0] | 0x0080 0000 |
| 0x29 | ch1_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2A | ch1_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2B | ch1_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2C | ch1_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2D | ch1_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2E | ch1_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2F | ch1_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

**Table 3. Serial Control Interface Register Summary (1) (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x30 | ch2_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x31 | ch2_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x32 | ch2_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x33 | ch2_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x34 | ch2_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x35 | ch2_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x36 | ch2_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x37 | ch6_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x38 | ch6_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x39 | | 4 | Reserved (3) | |

(3) Reserved registers should not be accessed.

**Table 3. Serial Control Interface Register Summary (1) (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x3A | DRC1 ae | 8 | u[31:26], ae[25:0] | 0x0080 0000 |
| | DRC1 (1 – ae) | | u[31:26], (1 – ae)[25:0] | 0x0000 0000 |
| 0x3B | DRC1 aa | 8 | u[31:26], aa[25:0] | 0x0080 0000 |
| | DRC1 (1 – aa) | | u[31:26], (1 – aa)[25:0] | 0x0000 0000 |
| 0x3C | DRC1 ad | 8 | u[31:26], ad[25:0] | 0x0080 0000 |
| | DRC1 (1 – ad) | | u[31:26], (1 – ad)[25:0] | 0x0000 0000 |
| 0x3D | DRC2 ae | 8 | u[31:26], ae[25:0] | 0x0080 0000 |
| | DRC 2 (1 – ae) | | u[31:26], (1 – ae)[25:0] | 0x0000 0000 |
| 0x3E | DRC2 aa | 8 | u[31:26], aa[25:0] | 0x0080 0000 |
| | DRC2 (1 – aa) | | u[31:26], (1 – aa)[25:0] | 0x0000 0000 |
| 0x3F | DRC2 ad | 8 | u[31:26], ad[25:0] | 0x0080 0000 |
| | DRC2 (1 – ad) | | u[31:26], (1 – ad)[27::0] | 0x0000 0000 |
| 0x40 | DRC1-T | 4 | T1[31:0] | 0xFDA2 1490 |
| 0x41 | DRC1-K | 4 | u[31:26], k1[25:0] | 0x0384 2109 |
| 0x42 | DRC1-O | 4 | u[31:24], O[23:16], O1[15:0] | 0x0008 4210 |
| 0x43 | DRC2-T | 4 | T2[31:0] | 0xFDA2 1490 |
| 0x44 | DRC2-K | 4 | u[31:24], k2'[22:0] | 0x0384 2109 |
| 0x45 | DRC2-O | 4 | u[31:24], O2[25:0] | 0x0008 4210 |
| 0x46 | DRC control | 4 | u[31:2], ch6[1], ch1_5[0] | 0x0000 0000 |
| 0x47–0x49 | | 4 | Reserved (4) | 0x0000 0000 |
| 0x50 | | 4 | Bank update command register | 0x0000 0000 |
| 0x51–0xFF | | 4 | Reserved (4) | 0x0000 0000 |

(4) Reserved registers should not be accessed.

## CLOCK CONTROL REGISTER (0x00)

In the manual mode, the clock control register provides a way for the system microprocessor to update the data and clock rates based on the sample rate and associated clock frequencies. In the auto-detect mode, the clocks are automatically determined by the TAS5706. In this case, the clock control register contains the auto-detected clock status as automatically detected (D7–D2). Bits D7–D5 selects the sample rate. Bits D4–D2 select the MCLK frequency. Bit D0 is used in manual mode only. In this mode, when the clocks are updated a 1 must be written to D0 to inform the DAP that the written clocks are valid.

**Table 4. Clock Control Register (0x00)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | – | – | – | – | – | $f_S$ = 32-kHz sample rate |
| 0 | 0 | 1 | – | – | – | – | – | $f_S$ = 38-kHz sample rate |
| 0 | 1 | 0 | – | – | – | – | – | $f_S$ = 44.1-kHz sample rate |
| **0** | **1** | **1** | **–** | **–** | **–** | – | **–** | **$f_S$ = 48-kHz sample rate (1)** |
| 1 | 0 | 0 | – | – | – | – | – | $f_S$ = 88.2-kHz sample rate |
| 1 | 0 | 1 | – | – | – | – | – | $f_S$ = 96-kHz sample rate |
| 1 | 1 | 0 | – | – | – | – | – | $f_S$ = 176.4-kHz sample rate |
| 1 | 1 | 1 | – | – | – | – | – | $f_S$ = 192-kHz sample rate |
| – | – | – | 0 | 0 | 0 | – | – | MCLK frequency = 64 × $f_S$ (2) |
| – | – | – | 0 | 0 | 1 | – | – | MCLK frequency = 128 × $f_S$ (3) |
| – | – | – | 0 | 1 | 0 | – | – | MCLK frequency = 192 × $f_S$ |

(1) Default values are in **bold**.
(2) Rate not available for 32-, 44.1-, and 48-kHz data rates
(3) Rate not available for 32-kHz data rate

**Table 4. Clock Control Register (0x00) (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **–** | **–** | **–** | **0** | **1** | **1** | **–** | **–** | **MCLK frequency = 256 × $f_S$** (1) |
| – | – | – | 1 | 0 | 1 | – | – | MCLK frequency = 384 × $f_S$ (4) |
| – | – | – | 1 | 1 | 0 | – | – | MCLK frequency = 512 × $f_S$ (4) |
| – | – | – | 1 | 1 | 1 | – | – | Reserved |
| – | – | – | – | – | – | – | – | Reserved |
| – | – | – | – | – | – | 1 | – | Bit clock (SCLK) frequency = 48 × $f_S$ (5) |
| – | – | – | – | – | – | **0** | – | **Bit clock (SCLK) frequency = 64 × $f_S$ or 32 × $f_S$ (selected in register 0x04)** (1) |
| **–** | **–** | **–** | – | **–** | **–** | **–** | **0** | **Clock not valid (in manual mode only)** (1) |
| – | – | – | | | | – | 1 | Clock valid (in manual mode only) |

(4) Rate not available for 176.4-kHz and 192-kHz data rates
(5) Rate only available for 192-$f_S$ and 384-$f_S$ MCLK frequencies

## DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the firmware revision.

**Table 5. General Status Register (0x01)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Default** (1) |
| – | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Identification code |

(1) Default values are in **bold**.

## ERROR STATUS REGISTER (0x02)

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if there are any persistent errors.

**Table 6. Error Status Register (0x02)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – | MCLK error |
| – | 1 | – | – | – | – | – | – | PLL autolock error |
| – | – | 1 | – | – | – | – | – | SCLK error |
| – | – | – | 1 | – | – | – | – | LRCLK error |
| – | – | – | – | 1 | – | – | – | Frame slip |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **No errors** (1) |

(1) Default values are in **bold**.

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if there are any persistent errors.

**Table 7. Error Status Register (0x02)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | 1 | – | – | – | – | – | – | PLL autolock error |
| – | – | 1 | – | – | – | – | – | SCLK error |
| – | – | – | 1 | – | – | – | – | LRCLK error |
| – | – | – | – | 1 | – | – | – | Frame slip |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **No errors** (1) |

(1) Default values are in **bold**.

## SYSTEM CONTROL REGISTER 1 (0x03)

The system control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled (default).

Bit D5: If 0, use soft unmute on recovery from clock error. This is a slow recovery.
If 1, use hard unmute on recovery from clock error (default). This is a fast recovery.

Bit D3: If 0, clock autodetect is enabled (default).
If 1, clock autodetect is disabled.

Bit D2: If 0, soft start is enabled (default).
If 1, soft start is disabled.

Bits D1–D0: Select de-emphasis

**Table 8. System Control Register 1 (0x03)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | – | – | – | – | – | – | – | PWM high-pass (dc blocking) disabled |
| **1** | – | – | – | – | – | – | – | **PWM high-pass (dc blocking) enabled** (1) |
| – | **0** | – | – | – | – | – | – | **Reserved** (1) |
| – | – | 0 | – | – | – | – | – | Soft unmute on recovery from clock error |
| – | – | **1** | – | – | – | – | – | **Hard unmute on recovery from clock error** (1) |
| – | – | – | **0** | – | – | – | – | **Reserved** (1) |
| – | – | – | – | **0** | – | – | – | **Enable clock autodetect** (1) |

(1) Default values are in **bold**.

**Table 8. System Control Register 1 (0x03) (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | 1 | – | – | – | Disable clock autodetect |
| – | – | – | – | – | **0** | – | – | **Enable soft start** (1) |
| – | – | – | – | – | 1 | – | – | Disable soft start |
| – | – | – | – | – | – | **0** | **0** | **No de-emphasis** (1) |
| – | – | – | – | – | – | 0 | 1 | Reserved |
| – | – | – | – | – | – | 1 | 0 | De-emphasis for $f_S$ = 44.1 kHz |
| – | – | – | – | – | – | 1 | 1 | De-emphasis for $f_S$ = 48 kHz |

## SERIAL DATA INTERFACE REGISTER (0x04)

As shown in , TAS5706 supports 21 serial data modes. The default is 24-bit, $I^2S$ mode,

**Serial Data Interface Control Register (0x04) Format**

| RECEIVE SERIAL DATA INTERFACE FORMAT | WORD LENGTH | D7–D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Right-justified | 16 | 000 | 0 | 0 | 0 | 0 | 0 |
| Right-justified | 20 | 000 | 0 | 0 | 0 | 0 | 1 |
| Right-justified | 24 | 000 | 0 | 0 | 0 | 1 | 0 |
| $I^2S$ | 16 | 000 | 0 | 0 | 0 | 1 | 1 |
| $I^2S$ | 20 | 000 | 0 | 0 | 1 | 0 | 0 |
| **$I^2S$** (1) | **24** | **000** | **0** | **0** | **1** | **0** | **1** |
| Left-justified | 16 | 000 | 0 | 0 | 1 | 1 | 0 |
| Left-justified | 20 | 000 | 0 | 0 | 1 | 1 | 1 |
| Left-justified | 24 | 000 | 0 | 1 | 0 | 0 | 0 |
| Reserved | | 000 | 0 | 1 | 0 | 0 | 1 |
| Right-justified | 18 | 000 | 0 | 1 | 0 | 1 | 0 |
| Reserved | | 000 | 0 | 1 | 0 | 1 | 1 |
| Reserved | | 000 | 0 | 1 | 1 | 0 | 0 |
| Reserved | | 000 | 0 | 1 | 1 | 0 | 1 |
| Reserved | | 000 | 0 | 1 | 1 | 1 | 0 |
| Reserved | | 000 | 0 | 1 | 1 | 1 | 1 |
| Reserved | | 000 | 1 | 0 | 0 | 0 | 0 |
| $I^2S$ (32 $f_S$ SCLK) | 16 | 000 | 1 | 0 | 0 | 1 | 1 |
| Left-justified (32 $f_S$ SCLK) | | 000 | 1 | 0 | 1 | 1 | 0 |
| Reserved | | 000 | 1 | 1 | 0 | 0 | 1 |
| Reserved | | 000 | 1 | 1 | 0 | 1 | 1 |
| Reserved | | 000 | 1 | 1 | 1 | 0 | 1 |

(1) Default values are in **bold**.

## SYSTEM CONTROL REGISTER 2 (0x05)

Bit D6 is a **control** bit and bit D5 is a **configuration** bit.

When bit D6 is set low, the system starts playing; otherwise, the outputs are shut down.

Bit D5 defines the configuration of the system, that is, it determines what configuration the system runs in when bit D6 is set low. When this bit is asserted, all channels are switching. Otherwise, only a subset of the PWM channels will run. The channels to shut down are defined in the shutdown group register (0x19). Bit D5 should only be changed when bit D6 is set, meaning that it is only possible to switch configurations by resetting the DAP and then restarting it again in the new configuration.

Bit D3 defines which volume register is used to control the volume of the HP_PWMx outputs when in headphone mode. When set to 0, the HP volume register (0x0C) controls the volume of the headphone outputs when in headphone mode. When bit D3 is set to 1, the channel volume registers (0x08–0x0B, 0x0D) are used for all modes (line out, headphone, speaker).

Bits D2–D1 define the output modes. The default is speaker mode with the headphone mode selectable via the external **HPSEL** terminal. The device can also be forced into headphone mode by asserting bit D1 (all other PWM channels are muted). Asserting bit D2 puts the device into a pseudo-line-out mode where the HP_PWMx and all other PWM channels are active. Bit D3 must also be asserted in this mode, and the HP_PWMx volume is controlled with the main speaker output volume controls via registers 0x08–0x0B and 0x0D..

**Table 9. System Control Register 2 (0x05)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved** (1) |
| – | 1 | 0 | – | – | – | – | – | All channels are shut down (hard mute). VALID1 = 0. |
| – | **1** | **1** | – | – | – | – | – | **All channels are shut down (hard mute). VALID1 = 0** (1) |
| – | 0 | 0 | – | – | – | – | – | When D6 is deasserted, all channels not belonging to shutdown group (SDG) are started. SDG register is 0x19. |
| – | 0 | 1 | – | – | – | – | – | When D6 is deasserted, all channels are started. VALID1 = 1. No channels in SDG1. |
| – | – | – | **0** | – | – | – | – | **Reserved** (2) |
| – | – | – | – | **0** | – | – | – | **Use HP volume register (0x0C) for adjusting headphone volume when in headphone mode.** (2) |
| – | – | – | – | 1 | – | – | – | Use channel volume registers (0x08–0x0B, 0x0D) for all modes. |
| – | – | – | – | – | **0** | **0** | – | **Speaker mode. Hardware pin, HPSEL = 1, forces device into headphone mode.** (2) |
| – | – | – | – | – | 0 | 1 | – | HP mode. This setting is logically ORed with external HPSEL pin. |
| – | – | – | – | – | 1 | 0 | – | Line out mode. Hardware pin, HPSEL, is ignored for this setting. HP_PWMx pins are active. |
| – | – | – | – | – | 1 | 1 | – | Reserved |
| – | – | – | – | – | – | – | **0** | **Reserved** (2) |

(1) Default values are in **bold**.
(2) Default values are in **bold**.

## SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle. Default is 0x00.

**Table 10. Soft Mute Register (0x06)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | 1 | Soft mute channel 1 |
| – | – | – | – | – | – | 1 | – | Soft mute channel 2 |
| – | – | – | – | – | 1 | – | – | Soft mute channel 3 |
| – | – | – | – | 1 | – | – | – | Soft mute channel 4 |
| – | – | 1 | – | – | – | – | – | Soft mute subwoofer channel (channel 6) |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | 0 | **Unmute all channels** (1) |

(1) Default values are in **bold**.

## VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D)

Step size is 0.5 dB.

| | |
|---|---|
| Master volume | – 0x07 (default is mute) |
| Channel-1 volume | – 0x08 (default is 0 dB) |
| Channel-2 volume | – 0x09 (default is 0 dB) |
| Channel-3 volume | – 0x0A (default is 0 dB) |
| Channel-4 volume | – 0x0B (default is 0 dB) |
| Headphone volume | – 0x0C (default is 0 dB) |
| Channel-6 volume (subwoofer) | – 0x0D (default is 0 dB) |

**Table 11. Volume Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 24 dB |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0 dB (default for individual channel volume) (1)** |
| | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | –100 dB |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **MUTE (default for master volume); 50% duty cycle at output – SOFT MUTE (1)** |

(1) Default values are in **bold**.

## VOLUME CONFIGURATION REGISTER (0x0E)

| | |
|---|---|
| Bit D7: | Reserved = 1 |
| Bit D6: | If 0, then biquad 1 (BQ1) volume compensation part only is disabled (default). If 1, then BQ1 volume compensation is enabled. |
| Bit D4: | Reserved = 1 |
| Bit D3: | Reserved |
| Bits D2–D0: | Volume slew rate (Used to control volume change and MUTE ramp rates) |

**Table 12. Volume Control Register (0x0E)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | – | – | – | – | – | – | – | **Reserved (must be 1)** |
| – | **0** | – | – | – | – | – | – | **Disable biquad volume compensation (1)** |
| – | 1 | – | – | – | – | – | – | Enable biquad volume compensation |
| – | – | **0** | – | – | – | – | – | **Reserved (1)** |
| – | – | – | **1** | – | – | – | – | **Reserved (must be 1) (1)** |
| – | – | – | – | **0** | – | – | – | **Reserved (1)** |
| – | – | – | – | – | 0 | 0 | 0 | Volume slew 512 steps (44 ms volume ramp time) |
| – | – | – | – | – | **0** | **0** | **1** | **Volume slew 1024 steps(1) (88 ms volume ramp time)** |
| – | – | – | – | – | 0 | 1 | 0 | Volume slew 2048 steps (176 ms volume ramp time) |
| – | – | – | – | – | 0 | 1 | 1 | Volume slew 256 steps (22 ms volume ramp time) |
| – | – | – | – | – | 1 | X | X | Reserved |

(1) Default values are in **bold**.

## MODULATION LIMIT REGISTER (0x10)

Set modulation limit. See the appropriate power stage data sheet for recommended modulation limits.

**Table 13. Modulation Limit Register (0x10)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | LIMIT [DCLKs] | MIN WIDTH [DCLKs] | MODULATION LIMIT |
|---|---|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | 0 | 0 | 0 | 1 | 2 | 99.2% |
| – | – | – | – | – | 0 | 0 | 1 | 2 | 4 | 98.4% |
| – | – | – | – | – | **0** | **1** | **0** | **3** | **6** | **97.7%** |
| – | – | – | – | – | 0 | 1 | 1 | 4 | 8 | 96.9% |
| – | – | – | – | – | 1 | 0 | 0 | 5 | 10 | 96.1% |
| – | – | – | – | – | 1 | 0 | 1 | 6 | 12 | 95.3% |
| – | – | – | – | – | 1 | 1 | 0 | 7 | 14 | 94.5% |
| – | – | – | – | – | 1 | 1 | 1 | 8 | 16 | 93.8% |

## INTERCHANNEL DELAY REGISTERS (0x11, 0x12, 0x13, 0x14, 0x15, 0x16)

Internal PWM Channels 1, 2, 3, 4, 5, and 6 are mapped into registers 0x11, 0x12 ,0x13, 0x14, 0x15, and 0x16.

**Table 14. Channel Interchannel Delay Register Format**

| BITS DEFINITION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Minimum absolute delay, 0 DCLK cycles, default for channel 0 (1)** |
| | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Maximum positive delay, 31 × 4 DCLK cycles |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Maximum negative delay, –32 × 4 DCLK cycles |
| | | | | | | | 0 | 0 | Unused bits |
| | | | | | | | | | |
| **SUBADDRESS** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Delay = (value) × 4 DCLKs** |
| **0x11** | **0** | **1** | **0** | **0** | **1** | **1** | **0** | **0** | **Default value for channel 1 (1) 19** |
| **0x12** | **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **Default value for channel 2 (1) 13** |
| **0x13** | **0** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **Default value for channel 3 (1) 7** |
| **0x14** | **0** | **1** | **1** | **0** | **0** | **1** | **0** | **0** | **Default value for channel 4 (1) 25** |
| **0x15** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **Default value for channel 5 (1) –12** |
| **0x16** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **Default value for channel 6 (1) -28** |

(1) Default values are in **bold**.

## OFFSET REGISTER (0x17)

The offset register is mapped into 0x17.

**Table 15. Channel Offset Register Format**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Minimum absolute offset, 0 DCLK cycles, default for channel 0 (1)** |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Maximum absolute offset, 255 DCLK cycles |

(1) Default values are in **bold**.

## PWM SHUTDOWN GROUP REGISTER (0x19)

Settings of this register determine which PWM channels are active. The default is 0x30 for two BTL output channels and no external subwoofer output. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

**Table 16. Shutdown Group Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved** (1) |
| – | **0** | – | – | – | – | – | – | **Reserved** (1) |
| – | – | **1** | – | – | – | – | – | **Channel 6 belongs to shut down group.** |
| – | – | 0 | – | – | – | – | – | Channel 6 does not belong to shutdown group. (1) |
| – | – | – | **1** | – | – | – | – | **Channel 5 belongs to shutdown group.** |
| – | – | – | 0 | – | – | – | – | Channel 5 does not belong to shutdown group. (1) |
| – | – | – | – | 1 | – | – | – | Channel 4 belongs to shutdown group. |
| – | – | – | – | **0** | – | – | – | **Channel 4 does not belong to shutdown group.** (1) |
| – | – | – | – | – | 1 | – | – | Channel 3 belongs to shutdown group. |
| – | – | – | – | – | **0** | – | – | **Channel 3 does not belong to shutdown group.** (1) |
| – | – | – | – | – | – | 1 | – | Channel 2 belongs to shutdown group. |
| – | – | – | – | – | – | **0** | – | **Channel 2 does not belong to shutdown group.** (1) |
| – | – | – | – | – | – | – | 1 | Channel 1 belongs to shutdown group. |
| – | – | – | – | – | – | – | **0** | **Channel 1 does not belong to shutdown group.** (1) |

(1) Default values are in **bold**.

## START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period when starting up or shutting down channels. The value in this register determines the time for which the PWM inputs switch at 50% duty cycle. This helps reduce pops and clicks at start-up and shutdown.

D7 is used to configure the output stage in a bridge-tied mode or a single-ended mode.

**Table 17. Start/Stop Period Register (0x1A)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Bridge-tied load (BTL)** |
| 1 | – | – | – | – | – | – | – | Single-ended load (SE) |
| – | – | – | 0 | 0 | – | – | – | No 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 0 | 0 | 16.5-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 0 | 1 | 23.9-ms 50% duty cycle start/stop period |
| – | – | – | **0** | **1** | **0** | **1** | **0** | **31.4-ms 50% duty cycle start/stop period** |
| – | – | – | 0 | 1 | 0 | 1 | 1 | 40.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 0 | 53.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 1 | 70.3-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 1 | 0 | 94.2-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 1 | 1 | 125.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 0 | 0 | 164.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 0 | 1 | 239.4-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 0 | 314.2-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 1 | 403.9-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 0 | 538.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 1 | 703.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 0 | 942.5-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 1 | 1256.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 0 | 1728.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 1 | 2513.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 0 | 3299.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 1 | 4241.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 0 | 5655.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 1 | 7383.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 0 | 9897.3-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 1 | 13,196.4-ms 50% duty cycle start/stop period |

## OSCILLATOR TRIM REGISTER (0x1B)

The TAS5706 PWM processor contains an internal oscillator for PLL reference. This reduces system cost because an external reference is not required. Currently, TI recommends a trim resistor value of 18.2 kΩ (1%). This should be connected between OSC_RES and DVSS.

The factory-trim procedure simply enables the factory trim that was previously done at the factory.

Note that trim always must be run following reset of the device.

### Oscillator Trim Enable Procedure Example

Write data 0x00 to register 0x1B (enable factory trim).

**Table 18. Oscillator Trim Register (0x1B)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | – | – | – | – | – | – | – | **Reserved** (1) |
| – | **0** | – | – | – | – | – | – | **Oscillator trim not done (read-only)** (1) |
| – | 1 | – | – | – | – | – | – | Oscillator trim done (read only) |
| – | – | **0** | **0** | **0** | **0** | – | – | **Reserved** (1) |
| – | – | – | – | – | – | 0 | – | Select factory trim (Write a 0 to select factory trim; default is 1.) |
| – | – | – | – | – | – | **1** | – | **Factory trim disabled** (1) |
| – | – | – | – | – | – | – | **0** | **Reserved** (1) |

(1) Default values are in **bold**.

## BKND_ERR REGISTER (0x1C)

When a back-end error signal is received ($\overline{\text{BKND\_ERR}}$ = LOW), all the output stages are reset by setting all PWM, VALID1, and VALID2 signals LOW. Subsequently, the modulator waits approximately for the time listed in Table 19 before initiation of a reset.

**Table 19. BKND_ERR Register (0x1C)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | 0 | 0 | 0 | 0 | Set back-end reset period to 0 ms (Reserved) |
| – | – | – | – | 0 | 0 | 0 | 1 | Set back-end reset period to 150 ms (Reserved) |
| – | – | – | – | **0** | **0** | **1** | **0** | **Set back-end reset period to 299 ms** (1) |
| – | – | – | – | 0 | 0 | 1 | 1 | Set back-end reset period to 449 ms |
| – | – | – | – | 0 | 1 | 0 | 0 | Set back-end reset period to 598 ms |
| – | – | – | – | 0 | 1 | 0 | 1 | Set back-end reset period to 748 ms |
| – | – | – | – | 0 | 1 | 1 | 0 | Set back-end reset period to 898 ms |
| – | – | – | – | 0 | 1 | 1 | 1 | Set back-end reset period to 1047 ms |
| – | – | – | – | 1 | 0 | 0 | 0 | Set back-end reset period to 1197 ms |
| – | – | – | – | 1 | 0 | 0 | 1 | Set back-end reset period to 1346 ms |
| – | – | – | – | 1 | 0 | 1 | 0 | Set back-end reset period to 1496 ms |
| – | – | – | – | 1 | 0 | 1 | 1 | Set back-end reset period to 1496 ms |
| – | – | – | – | 1 | 1 | – | – | Set back-end reset period to 1496 ms |

(1) Default values are in **bold**.

## INPUT MULTIPLEXER REGISTER (0x20)

The hex value for each nibble is the channel number. For each input multiplexer, any input from SDIN1, SDIN2 can be mapped to any internal TAS5706 channel.

**Table 20. Input Multiplexer Register (0x20)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved = 0x00** |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| 0 | – | – | – | – | – | – | – | Channel-1 AD mode |
| **1** | – | – | – | – | – | – | – | **Channel-1 BD mode** (1) |
| – | **0** | **0** | **0** | – | – | – | – | **SDIN1-L to channel 1** (1) |
| – | 0 | 0 | 1 | – | – | – | – | SDIN1-R to channel 1 |
| – | 0 | 1 | 0 | – | – | – | – | SDIN2-L to channel 1 |
| – | 0 | 1 | 1 | – | – | – | – | SDIN2-R to channel 1 |
| – | 1 | 0 | 0 | – | – | – | – | Reserved |
| – | 1 | 0 | 1 | – | – | – | – | Reserved |
| – | 1 | 1 | 0 | – | – | – | – | Ground (0) to channel 1 |
| – | 1 | 1 | 1 | – | – | – | – | Reserved |
| – | – | – | – | 0 | – | – | – | Channel 2 AD mode |
| – | – | – | – | **1** | – | – | – | **Channel 2 BD mode** (1) |
| – | – | – | – | – | 0 | 0 | 0 | SDIN1-L to channel 2 |
| – | – | – | – | – | **0** | **0** | **1** | **SDIN1-R to channel 2** (1) |
| – | – | – | – | – | 0 | 1 | 0 | SDIN2-L to channel 2 |
| – | – | – | – | – | 0 | 1 | 1 | SDIN2-R to channel 2 |
| – | – | – | – | – | 1 | 0 | 0 | Reserved |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | 0 | Ground (0) to channel 2 |
| – | – | – | – | – | 1 | 1 | 1 | Reserved |

(1) Default values are in **bold**.

**Table 20. Input Multiplexer Register (0x20) (continued)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved** |
| – | 0 | 0 | 0 | – | – | – | – | SDIN1-L to channel 3 |
| – | 0 | 0 | 1 | – | – | – | – | SDIN1-R to channel 3 |
| – | 0 | 1 | 0 | – | – | – | – | SDIN2-L to channel 3 |
| – | 0 | 1 | 1 | – | – | – | – | SDIN2-R to channel 3 |
| – | 1 | 0 | 0 | – | – | – | – | Reserved |
| – | 1 | 0 | 1 | – | – | – | – | Reserved |
| – | 1 | 1 | 0 | – | – | – | – | Ground (0) to channel 3 |
| – | **1** | **1** | **1** | – | – | – | – | **Ch1 (BTL–) to channel 3—BTL pair for channel 1** (2) |
| – | – | – | – | **0** | – | – | – | **Reserved** (2) |
| – | – | – | – | – | 0 | 0 | 0 | SDIN1-L to channel 4 |
| – | – | – | – | – | 0 | 0 | 1 | SDIN1-R to channel 4 |
| – | – | – | – | – | 0 | 1 | 0 | SDIN2-L to channel 4 |
| – | – | – | – | – | 0 | 1 | 1 | SDIN2-R to channel 4 |
| – | – | – | – | – | 1 | 0 | 0 | Reserved |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | 0 | Ground (0) to channel 4 |
| – | – | – | – | – | **1** | **1** | **1** | **Ch2 (BTL–) to channel 4—BTL pair for channel 2** (2) |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved** |
| – | 1 | 0 | 0 | – | – | – | – | Reserved |
| – | 1 | 0 | 1 | – | – | – | – | Reserved |
| – | 1 | 1 | 0 | – | – | – | – | Ground (0) to channel 5 |
| **–** | **1** | **1** | **1** | – | – | – | – | **Ch6 (BTL–) to channel 5—BTL pair to channel 6** |
| – | – | – | – | 0 | – | – | – | Channel 6 AD mode (2) |
| – | – | – | – | **1** | – | – | – | **Channel 6 BD mode** |
| – | – | – | – | – | 0 | 0 | 0 | SDIN1-L to channel 6 |
| – | – | – | – | – | 0 | 0 | 1 | SDIN1-R to channel 6 |
| – | – | – | – | – | **0** | **1** | **0** | **SDIN2-L to channel 6** (2) |
| – | – | – | – | – | 0 | 1 | 1 | SDIN2-R to channel 6 |
| – | – | – | – | – | 1 | 0 | 0 | Reserved |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | 0 | Ground (0) to channel 6 (2) |
| – | – | – | – | – | 1 | 1 | 1 | Reserved |

(2) Default values are in **bold**.

## DOWNMIX INPUT MULTIPLEXER REGISTER (0x21)

| | |
|---|---|
| Bits D31–D16: | Unused |
| Bits D15–D13: | Reserved |
| Bit D12: | If 1, selects downmix data L' to internal channel L<br>If 0, selects channel 1 data (from input mux 1) to DAP internal channel 1 |
| Bit D11: | If 1, selects downmix data R' to the DAP internal channel 2<br>If 0, selects channel 2 data (from input mux 2) to DAP internal channel 2 |
| Bits D10–D8: | Reserved |
| Bits D7–D3: | Reserved |
| Bit D1: | If 1, enable data from input mux 2 to downmix block<br>If 0, disable data from input mux 2 to downmix block |
| Bit D0: | If 1, enable data from input mux 1 to downmix block<br>If 0, disable data from input mux 1 to downmix block |

**Table 21. Downmix Input Multiplexer Register**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – | Unused |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| – | – | – | – | – | – | – | – | Unused |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **1** | **0** | – | – | – | – | – | **Reserved** (1) |
| – | – | – | 1 | – | – | – | – | Enable downmix data L' to channel 1 |
| – | – | – | **0** | – | – | – | – | **Enable channel 1 data to channel 1** (1) |
| – | – | – | – | 1 | – | – | – | Enable downmix data R' to channel 2 |
| – | – | – | – | **0** | – | – | – | **Enable channel 2 data to channel 2** (1) |
| – | – | – | – | – | **0** | – | – | Reserved |
| – | – | – | – | – | – | 0 | 0 | Enable channel 6 data to channel 6 |
| – | – | – | – | – | – | 0 | 1 | Enable bass management on channel 6 |
| – | – | – | – | – | – | **1** | 0 | **Enable (L'+R')/2 downmix data on channel 6** (1) |
| – | – | – | – | – | – | 1 | 1 | Reserved |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| – | – | – | – | – | – | – | **1** | **Enable data from input multiplexer 1 to downmix block** (1) |
| – | – | – | – | – | – | – | 0 | Disable data from input multiplexer 1 to downmix block |
| – | – | – | – | – | – | **1** | – | **Enable data from input multiplexer 2 to downmix block** (1) |
| – | – | – | – | – | – | 0 | – | Disable data from input multiplexer 2 to downmix block |
| **0** | **0** | **0** | **0** | **0** | **0** | – | – | **Reserved** (1) |

(1) Default values are in **bold**.

## AM MODE REGISTER (0x22)

See the *PurePath Digital™ AM Interference Avoidance* application note (SLEA040).

**Table 22. AM Mode Register (0x22)**

| D20 | D19 | D18 | D17 | D16 | FUNCTION |
|---|---|---|---|---|---|
| **0** | – | – | – | – | **AM mode disabled** (1) |
| 1 | – | – | – | – | AM mode enabled |
| – | **0** | **0** | – | – | **Select sequence 1** (1) |
| – | 0 | 1 | – | – | Select sequence 2 |
| – | 1 | 0 | – | – | Select sequence 3 |
| – | 1 | 1 | – | – | Select sequence 4 |
| – | – | – | **0** | – | **IF frequency = 455 kHz** (1) |
| – | – | – | 1 | – | IF frequency = 262.5 kHz |
| – | – | – | – | **0** | **Use BCD tuned frequency** (1) |
| – | – | – | – | 1 | Use binary tuned frequency |

(1) Default values are in **bold**.

**Table 23. AM Tuned Frequency Register in BCD Mode**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | X | – | – | – | – | BCD frequency (1000s kHz) |
| – | – | – | – | X | X | X | X | BCD frequency (100s kHz) |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Default value** (1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | – | – | – | – | BCD frequency (10s kHz) |
| – | – | – | – | X | X | X | X | BCD frequency (1s kHz) |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Default value** (1) |

(1) Default values are in **bold**.

OR

**Table 24. AM Tuned Frequency Register in Binary Mode**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | X | X | X | Binary frequency |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Default value** (1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| X | X | X | X | X | X | X | X | Binary frequency |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Default value** (1) |

(1) Default values are in **bold**.

## PWM OUTPUT MUX REGISTER (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D30–D25: Selects which PWM channel is output to HPL_PWM and HPR_PWM

Bits D23–D20: Selects which PWM channel is output to OUT_A

Bits D19–D16: Selects which PWM channel is output to OUT_B

Bits D15–D12: Selects which PWM channel is output to OUT_C

Bits D11–D08: Selects which PWM channel is output to OUT_D

Bits D07–D04: Selects which PWM channel is output to SUB_PWM–

Bits D03–D00: Selects which PWM channel is output to SUB_PWM+

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 6 = 0x05.

**Table 25. PWM Output Mux Register (0x25)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved** (1) |
| – | **0** | **0** | **0** | – | – | – | – | **Multiplex channel 1 to HPL_PWM** (1) |
| – | 0 | 0 | 1 | – | – | – | – | Multiplex channel 2 to HPL_PWM |
| – | 0 | 1 | 0 | – | – | – | – | Multiplex channel 3 to HPL_PWM |
| – | 0 | 1 | 1 | – | – | – | – | Multiplex channel 4 to HPL_PWM |
| – | 1 | 0 | 0 | – | – | – | – | Multiplex channel 5 to HPL_PWM |
| – | 1 | 0 | 1 | – | – | – | – | Multiplex channel 6 to HPL_PWM |
| – | – | – | – | **0** | – | – | – | **Reserved** |
| – | – | – | – | – | 0 | 0 | 0 | Multiplex channel 1 to HPR_PWM |
| – | – | – | – | – | **0** | **0** | **1** | **Multiplex channel 2 to HPR_PWM** (1) |
| – | – | – | – | – | 0 | 1 | 0 | Multiplex channel 3 to HPR_PWM |
| – | – | – | – | – | 0 | 1 | 1 | Multiplex channel 4 to HPR_PWM |
| – | – | – | – | – | 1 | 0 | 0 | Multiplex channel 5 to HPR_PWM |
| – | – | – | – | – | 1 | 0 | 1 | Multiplex channel 6 to HPR_PWM |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | **0** | **0** | – | – | – | – | **Multiplex channel 1 to OUT_A** (1) |
| 0 | 0 | 0 | 1 | – | – | – | – | Multiplex channel 2 to OUT_A |
| 0 | 0 | 1 | 0 | – | – | – | – | Multiplex channel 3 to OUT_A |
| 0 | 0 | 1 | 1 | – | – | – | – | Multiplex channel 4 to OUT_A |
| 0 | 1 | 0 | 0 | – | – | – | – | Multiplex channel 5 to OUT_A |
| 0 | 1 | 0 | 1 | – | – | – | – | Multiplex channel 6 to OUT_A |
| – | – | – | – | 0 | 0 | 0 | 0 | Multiplex channel 1 to OUT_B |
| – | – | – | – | 0 | 0 | 0 | 1 | Multiplex channel 2 to OUT_B |
| – | – | – | – | **0** | **0** | **1** | **0** | **Multiplex channel 3 to OUT_B** (1) |
| – | – | – | – | 0 | 0 | 1 | 1 | Multiplex channel 4 to OUT_B |
| – | – | – | – | 0 | 1 | 0 | 0 | Multiplex channel 5 to OUT_B |
| – | – | – | – | 0 | 1 | 0 | 1 | Multiplex channel 6 to OUT_B |

(1) Default values are in **bold**.

**Table 25. PWM Output Mux Register (0x25) (continued)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| 0 | 0 | 0 | 0 | – | – | – | – | Multiplex channel 1 to OUT_C |
| **0** | **0** | **0** | **1** | – | – | – | – | **Multiplex channel 2 to OUT_C** (2) |
| 0 | 0 | 1 | 0 | – | – | – | – | Multiplex channel 3 to OUT_C |
| 0 | 0 | 1 | 1 | – | – | – | – | Multiplex channel 4 to OUT_C |
| 0 | 1 | 0 | 0 | – | – | – | – | Multiplex channel 5 to OUT_C |
| 0 | 1 | 0 | 1 | – | – | – | – | Multiplex channel 6 to OUT_C |
| – | – | – | – | 0 | 0 | 0 | 0 | Multiplex channel 1 to OUT_D |
| – | – | – | – | 0 | 0 | 0 | 1 | Multiplex channel 2 to OUT_D |
| – | – | – | – | 0 | 0 | 1 | 0 | Multiplex channel 3 to OUT_D |
| – | – | – | – | **0** | **0** | **1** | **1** | **Multiplex channel 4 to OUT_D** (2) |
| – | – | – | – | 0 | 1 | 0 | 0 | Multiplex channel 5 to OUT_D |
| – | – | – | – | 0 | 1 | 0 | 1 | Multiplex channel 6 to OUT_D |
| | | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
| 0 | 0 | 0 | 0 | – | – | – | | Multiplex channel 1 to SUB_PWM– |
| 0 | 0 | 0 | 1 | – | – | – | – | Multiplex channel 2 to SUB_PWM– |
| 0 | 0 | 1 | 0 | – | – | – | – | Multiplex channel 3 to SUB_PWM– |
| 0 | 0 | 1 | 1 | – | – | – | – | Multiplex channel 4 to SUB_PWM– |
| **0** | **1** | **0** | **0** | – | – | – | – | **Multiplex channel 5 to SUB_PWM–** (2) |
| 0 | 1 | 0 | 1 | – | – | – | – | Multiplex channel 6 to SUB_PWM– |
| – | – | – | – | 0 | 0 | 0 | 0 | Multiplex channel 1 to SUB_PWM+ |
| – | – | – | – | 0 | 0 | 0 | 1 | Multiplex channel 2 to SUB_PWM+ |
| – | – | – | – | 0 | 0 | 1 | 0 | Multiplex channel 3 to SUB_PWM+ |
| – | – | – | – | 0 | 0 | 1 | 1 | Multiplex channel 4 to SUB_PWM+ |
| – | – | – | – | 0 | 1 | 0 | 0 | Multiplex channel 5 to SUB_PWM+ |
| – | – | – | – | **0** | **1** | **0** | **1** | **Multiplex channel 6 to SUB_PWM+** (2) |

(2) Default values are in **bold**.

## LOUDNESS BIQUAD GAIN INVERSE REGISTER (0x26)

Bit D6 of the volume configuration register (0x0E) enables/disables gain compensation for BQ1. D6 = 0 disables gain compensation (default); D6 = 1 enables gain compensation. Max/min biquad gain = ±4.

**Table 26. Loudness Biquad Gain Inverse Register (3.23 Format)**

| CONTENT | DEFINITION |
|---|---|
| u[31:26], x[25:0] | 1/G (1) |

(1) G = gain of the biquad

## LOUDNESS SCALE REGISTER (0x28)

**Table 27. Loudness Scale Register (3.23 Format)**

| CONTENT | DEFINITION |
|---|---|
| u[31:26], x[25:0] | Scale = 1/(1 – 1/G) (1) |

(1) G = gain of the biquad

## DRC CONTROL (0x46)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | **0** | **DRC1 (satellite channels) turned OFF** (1) |
| – | – | – | – | – | – | – | 1 | DRC1 (satellite channels) turned ON |
| – | – | – | – | – | – | **0** | – | **DRC2 (subchannel ) turned OFF** (1) |
| – | – | – | – | – | – | 1 | – | DRC2 (subchannel ) turned ON |
| – | – | – | – | – | **0** | – | – | **DRC1 independent of channel 3** (1) |
| – | – | – | – | – | 1 | – | – | DRC1 dependent of channel 3 |
| – | – | – | – | **0** | – | – | – | **DRC1 independent of channel 4** (1) |
| – | – | – | – | 1 | – | – | – | DRC1 dependent of channel 4 |

(1) Default values are in **bold**.

## BANK SWITCH AND HEADPHONE DRC/EQ CONTROL (0x50)

### Table 28. Bank Switching Command

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| – | – | – | – | – | **0** | **0** | **0** | **No bank switching. All updates to DAP** (1) |
| – | – | – | – | – | 0 | 0 | 1 | Configure bank 1 (32 kHz) |
| – | – | – | – | – | 0 | 1 | 0 | Configure bank 2 (44.1/48 kHz) |
| – | – | – | – | – | 0 | 1 | 1 | Configure bank 3 (88.2/96 kHz and above) |
| – | – | – | – | – | 1 | 0 | 0 | Automatic bank selection |
| – | – | **0** | **0** | **0** | – | – | – | **Reserved** |
| – | **0** | – | – | – | – | – | – | **DRC disabled in headphone mode** (1) |
| – | 1 | – | – | – | – | – | – | DRC enabled in headphone mode |
| **0** | – | – | – | – | – | – | – | **EQ disabled in headphone mode** (1) |
| 1 | – | – | – | – | – | – | – | EQ enabled in headphone mode |

(1) Default values are in **bold**.

# REVISION HISTORY

**Changes from Revision A (December 2007) to Revision B** **Page**

- Changed description for AVDD pin ..... 7
- Changed description for DVDD pin ..... 8
- Added start-up sequence to data sheet ..... 40
- Added *Start-Up Sequence* timing diagram to data sheet ..... 42

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5706PAP | ACTIVE | HTQFP | PAP | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 0 to 85 | TAS5706 | Samples |
| TAS5706PAPR | ACTIVE | HTQFP | PAP | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 0 to 85 | TAS5706 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

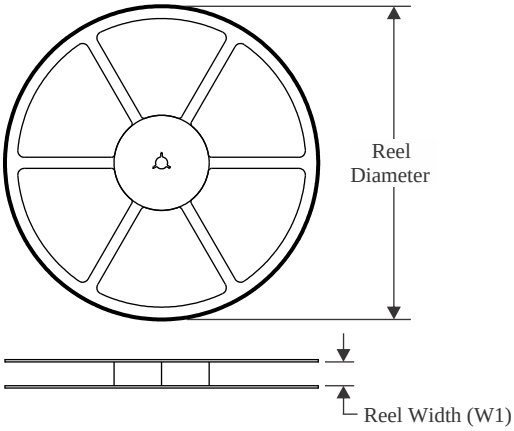
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

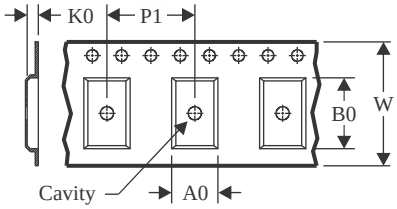
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

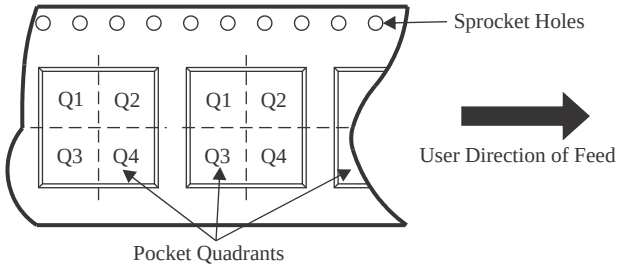



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

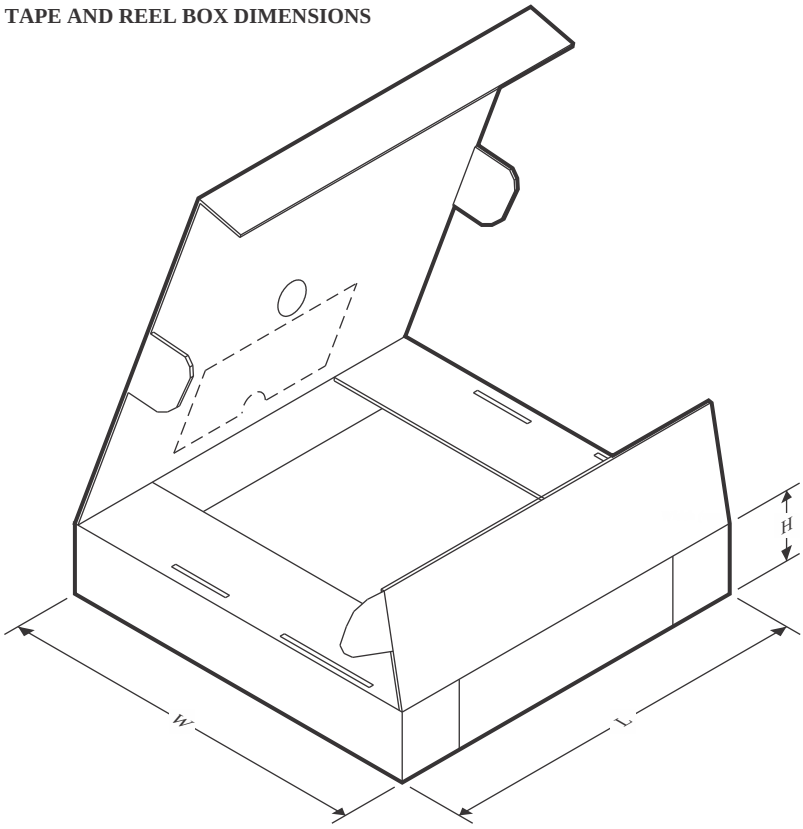
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5706PAPR | HTQFP | PAP | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |

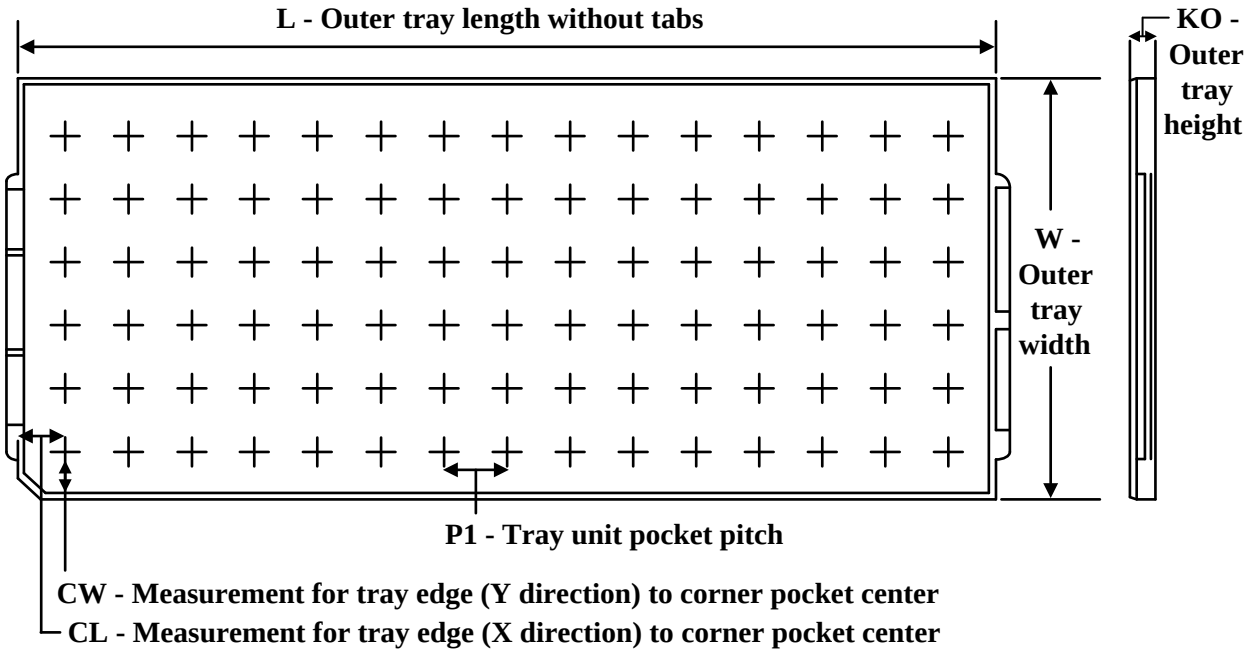
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TAS5706PAPR | HTQFP | PAP | 64 | 1000 | 350.0 | 350.0 | 43.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5706PAP | PAP | HTQFP | 64 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |

# GENERIC PACKAGE VIEW

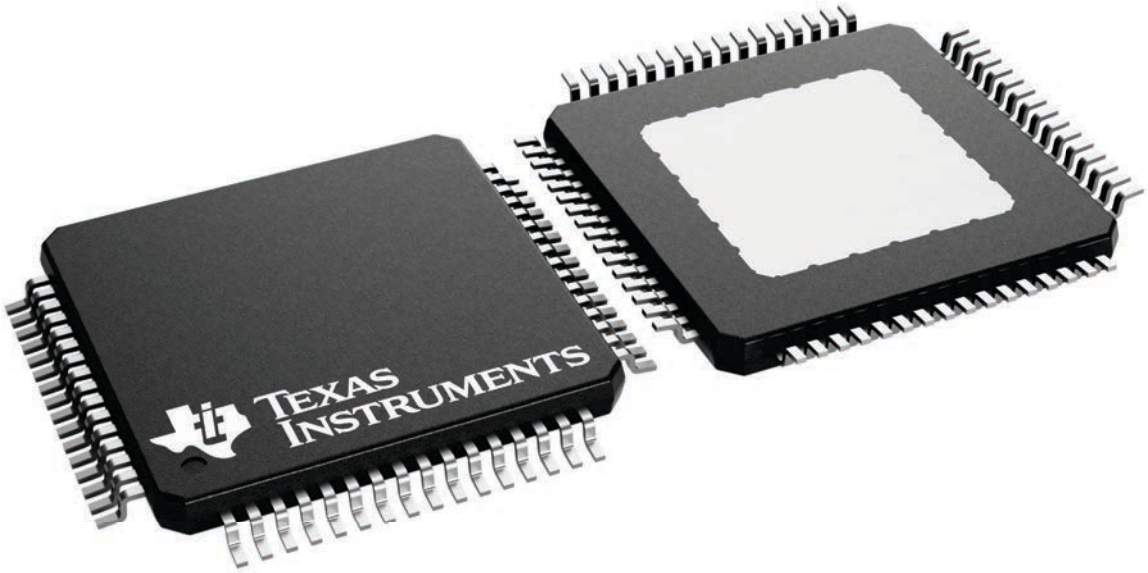
## PAP 64

## HTQFP - 1.2 mm max height

**10 x 10, 0.5 mm pitch**

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



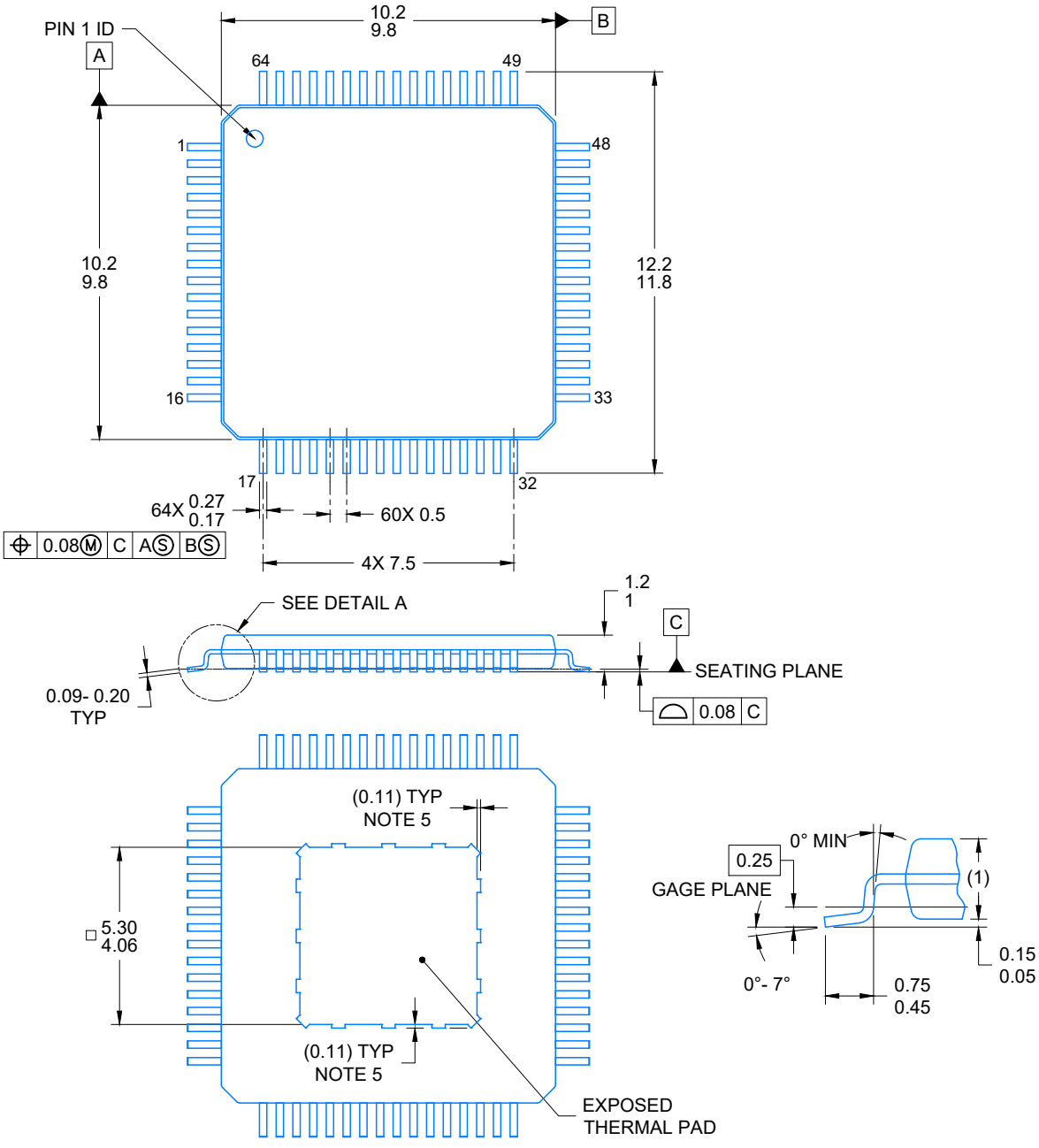

4226442/A

# PACKAGE OUTLINE

## PAP0064N

## HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK




4225982/B 07/2021

NOTES:

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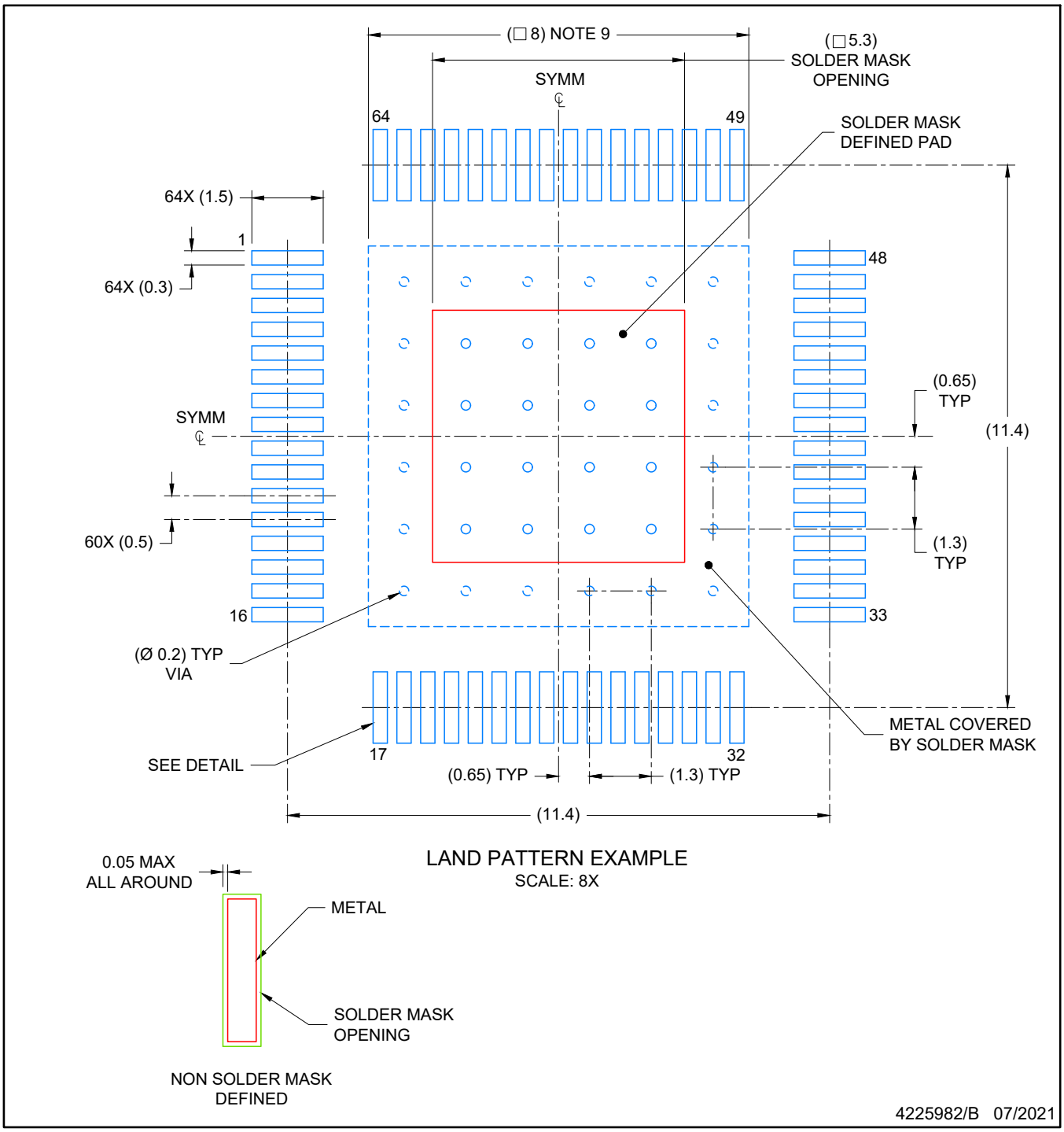
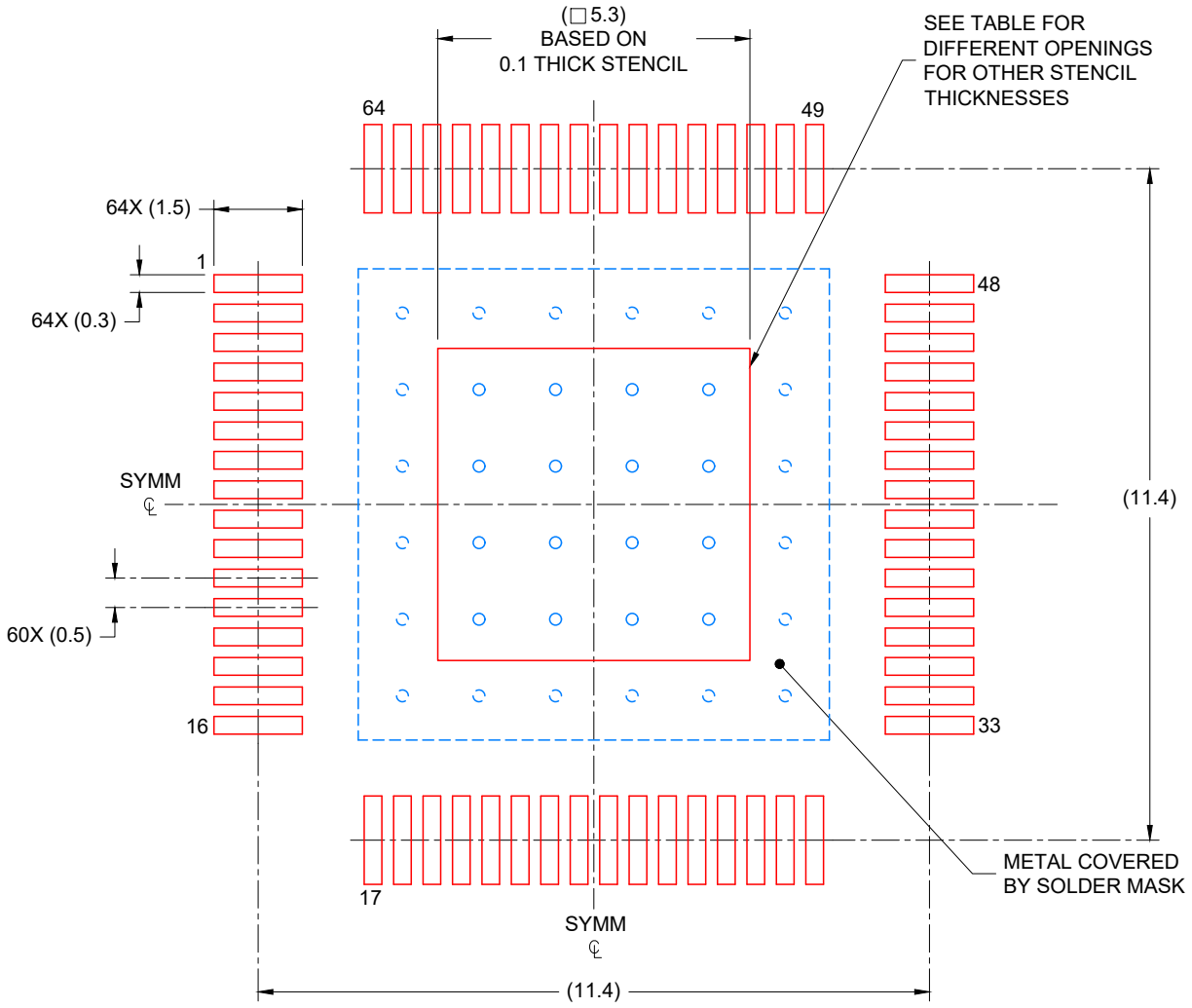
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Strap features may not be present.
6. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED COVERAGE BY AREA
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 5.3X5.3 (SHOWN) |
| 0.127 | 4.44 X 4.44 |
| 0.152 | 4.06 X 4.06 |
| 0.178 | 3.75 X 3.75 |

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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